PC SDRAM Registered DIMM Specification

REVISION 1.0

February, 1998

The information in this document is subject to change.

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REVISION HISTORY

Revision 0.80: December 1997

- Added post register timing information
- Add PLL critical specifications
- Add register critical specifications
- Corrected register part numbers
- Updated post register timing information
- Added new 256MB Topology information
- Added preliminary information on the 64MB DIMM without the PLL
- Added preliminary information on adapting the spec for 512MB DIMM

Revision 1.00: February 1998

- Updated Introduction section
- Updated information for the 64MB DIMM without the PLL
- Updated all topology and component value tables
- Corrected PLL part numbers
- Modified PLL component requirements to support SSC synthesizers
- Added VI curves for the Register and PLL

1. Introduction

This specification defines the electrical and mechanical requirements for 168-pin, 3.3 volt, 100 MHz, 72-bit wide, 4 clock, Registered Synchronous DRAM Dual In-Line Memory Modules (SDRAM DIMMs). These SDRAM DIMMs are intended for use as main memory when installed on personal computer motherboards.

A reference design example is documented in this specification. The reference design is intended to provide an initial basis for a registered DIMM design. Modifications to this reference design may be required to meet all system timing, signal integrity and thermal requirements for 100MHz support. All registered DIMM implementations must use simulations and lab verification to insure proper timing requirements and signal integrity in the design.

This specification for 256MB and 512MB registered DIMMs is generated using a stacked SDRAM package implementation. Other SDRAM packaging implementations may need to deviate from this specification.

This specification largely follows the JEDEC defined 168-pin 8-Byte Registered SDRAM DIMM Product Overview as of JEDEC committee meeting of December 1996 (document number JC-42.5-96-146A).

Related Documents

Table 1: Related Documents

TITLE	REV
Intel PC SDRAM Specification	Latest Revision
Intel PC SDRAM SPD Data Structure Specification	Latest Revision

DIMM Configurations

SDRAM DIMM configurations are defined in the following table:

Table 2: SDRAM Module Configurations

Config #	DIMM Capacity	DIMM Organization	SDRAM density	SDRAM Organization	# of SDRAMs	# Rows of SDRAM	# Banks in SDRAM	# Address bits row/bank/col
1	64 MB	8M X 72	64Mbit	8M X 8	9	1	4	12/2/9
2	128 MB	16M X 72	64Mbit	16M X 4	18	1	4	12/2/10
3	256 MB	32M X 72	64Mbit	16M X 4	36	2	4	12/2/10
4	512MB	64M X 72	128Mbit	32M x 4	36	2	4	12/2/11

Note: All references in this specification to the 256MB implementation also refer to the 512MB implementation.

2. Environmental Requirements

The Registered SDRAM DIMM shall be designed to operate within a personal computer cabinet in an office environment with limited capacity for heating and air conditioning. The temperature and humidity limits are listed below.

Table 3: DIMM Temperature, Humidity & Barometric Pressure Requirements

Operating Temperature	0 ^{o}C to +55 ^{o}C ambient
Operating Humidity	10% to 90% relative humidity
Storage Temperature	-50 ^{o}C to + 100 ^{o}C
Storage Humidity	5% to 95% without condensation
Barometric Pressure (operating & storage)	105K - 69K Pascal (up to 9,850 ft.)

3. Mechanical Design

The following table and mechanical drawings give the specific dimensions and tolerances for a 168-pin Registered DIMM.

Table 4: DIMM Dimensions and Tolerances

SYMBOL	DEFINITION	MIN	NOM	MAX	NOTES
A	Overall module height measured from Datum -B-.		38.12 mm	43.18 mm	Nominal is 38.10 mm. (1.5”). Max is 43.18 (1.7”).
A1	The distance from Datum -B- to the centerline of the PWB alignment holes.	3.00 mm BASIC			These holes are not used by the next level of assembly. The dimensions are supplied for information only. If the holes are used in manufacturing they should be tightly toleranced. The recommended positional tolerance is 0.10 mm.
A2	The distance from Datum -B- to the centerline of the latch holes.	17.80 mm BASIC			
A3	The distance from Datum -B- to the lower edge of the Component Area.	20.80 mm			This distance applies to the Component Area in the latch hole area.
A4	The distance from Datum -B- to the lower edge of the Component Area on the front side of the PWB.	4.00 mm			
A5	The distance from Datum -B- to the lower edge of the Component Area on the back side of the PWB.	4.00 mm			
A6	The distance from Datum -B- to the leading edge of the contact.	0.05 mm		0.35 mm	The minimum distance prevents contact edge burrs.
b	The width of the plated input/output contact measured at the lateral midpoint of the contact.	0.95 mm	1.00 mm	1.05 mm	
D1	The overall length of the PWB.	133.22 mm	133.37 mm	133.52 mm	
D2	The longitudinal distance between the PWB machining alignment hole centers.	126.20 mm	127.35	128.50 mm	These holes are optional and may or may not be present. If they are present, they must be located as defined.

Table 5: DIMM Dimensions and Tolerances (continued)

SYMBOL	DEFINITION	MIN	NOM	MAX	NOTES
e	The pitch or distance between centerlines of the contacts	1.27 mm BASIC			
e1	The distance between the centerlines of Contact 1 and 84.		115.57 mm		
e2	The distance between the centerlines of Contact 85 and 168.		115.57 mm		
e3	The distance between the centerlines of Contact 1 and the contact located at the immediate left of the left key zone when viewing contact 1 side.		11.43 mm		The distance between the centerlines of contact 1 and 10.
e4	The distance between the centerlines of the contact at the immediate right of the left key zone and the contact at the immediate left of the center key zone when viewing contact 1 side.		36.83 mm		The distance between the centerlines of contact 11 and 40.
e5	The distance between the centerlines of the contact located at the immediate right of the center key zone and contact 84.		54.61 mm		The distance between the centerlines of contact 41 and 84.
H	The diameter of the PWB machined alignment holes.	2.90 mm	3.00 mm	3.10 mm	The machined alignment holes are optional.
L	The distance from Datum -B- to the top edge of the plated contact.	2.30 mm	2.50 mm	2.70 mm	
N	The total number of contacts.		168		
T	The thickness of the PCB including the contact metalization and plating.	1.17 mm	1.27 mm	1.37 mm	
T1	The overall thickness of the PWB with the components mounted. The overall thickness is measured from the highest component on the front side to the highest component on the backside.			8.13 mm	
aaa	The positional tolerance for the overall body length D1.	aaa = 0.15 mm @ Maximum Material Condition			
bbb	The straightness tolerance for the card thickness including the metalized contacts. This callout applies to the zone defined by A4, A5 and D1.		0.40 mm		bbb = 0.3% x D1 rounded to a two decimal place hard metric value.
ccc	The positional tolerance for the pattern of contacts with regard to primary Datum -A-.	ccc = 0.10 mm @ Least Material Condition			
ddd	The positional tolerance for the individual contact width b with regard to the theoretical centerline of the contact defined by basic dimension e.	ddd = 0.05 mm @ Least Material Condition			

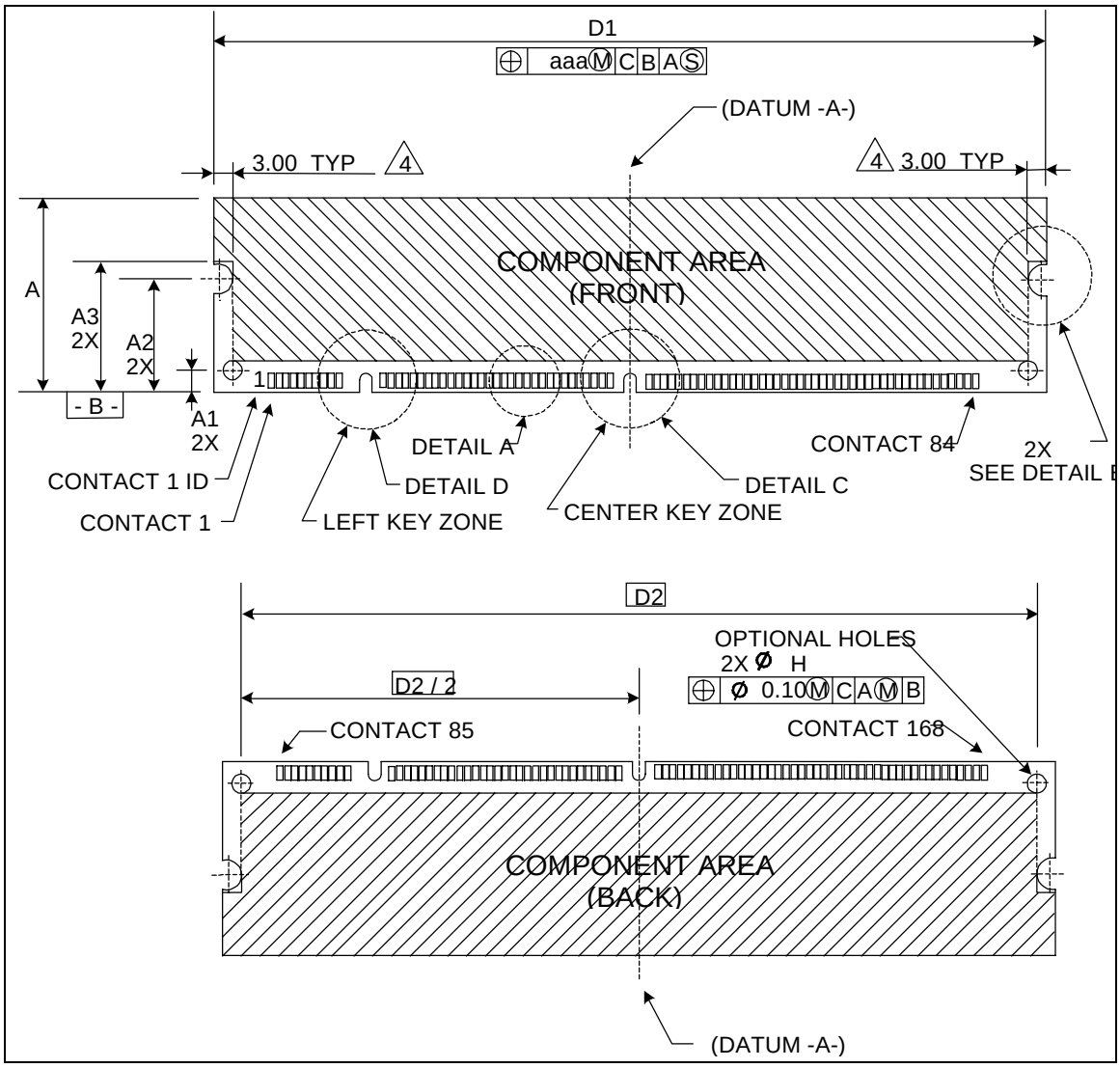


Figure 1: DIMM Mechanical Drawing (1 of 5)

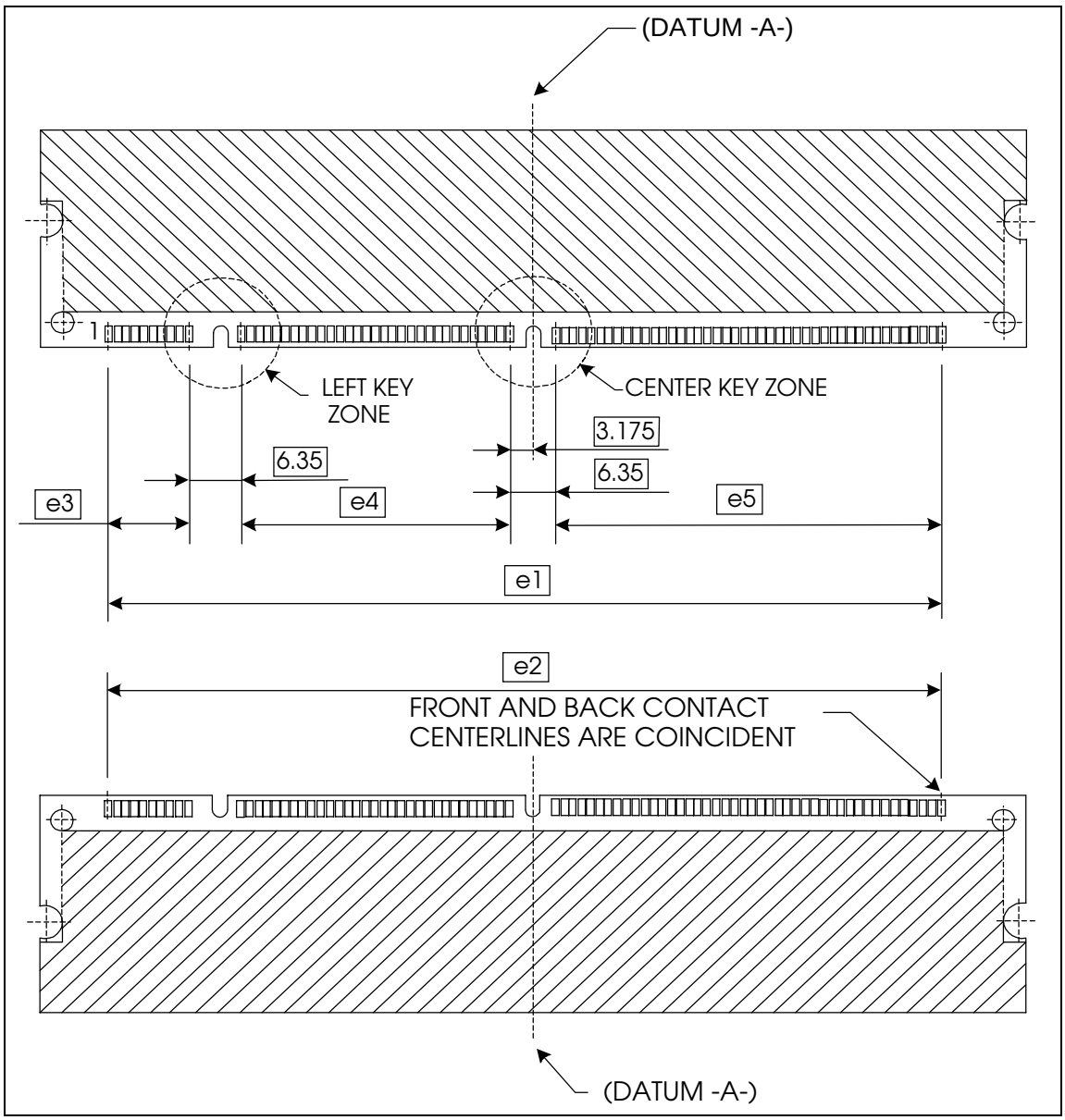


Figure 2: DIMM Mechanical Drawing (2 of 5)

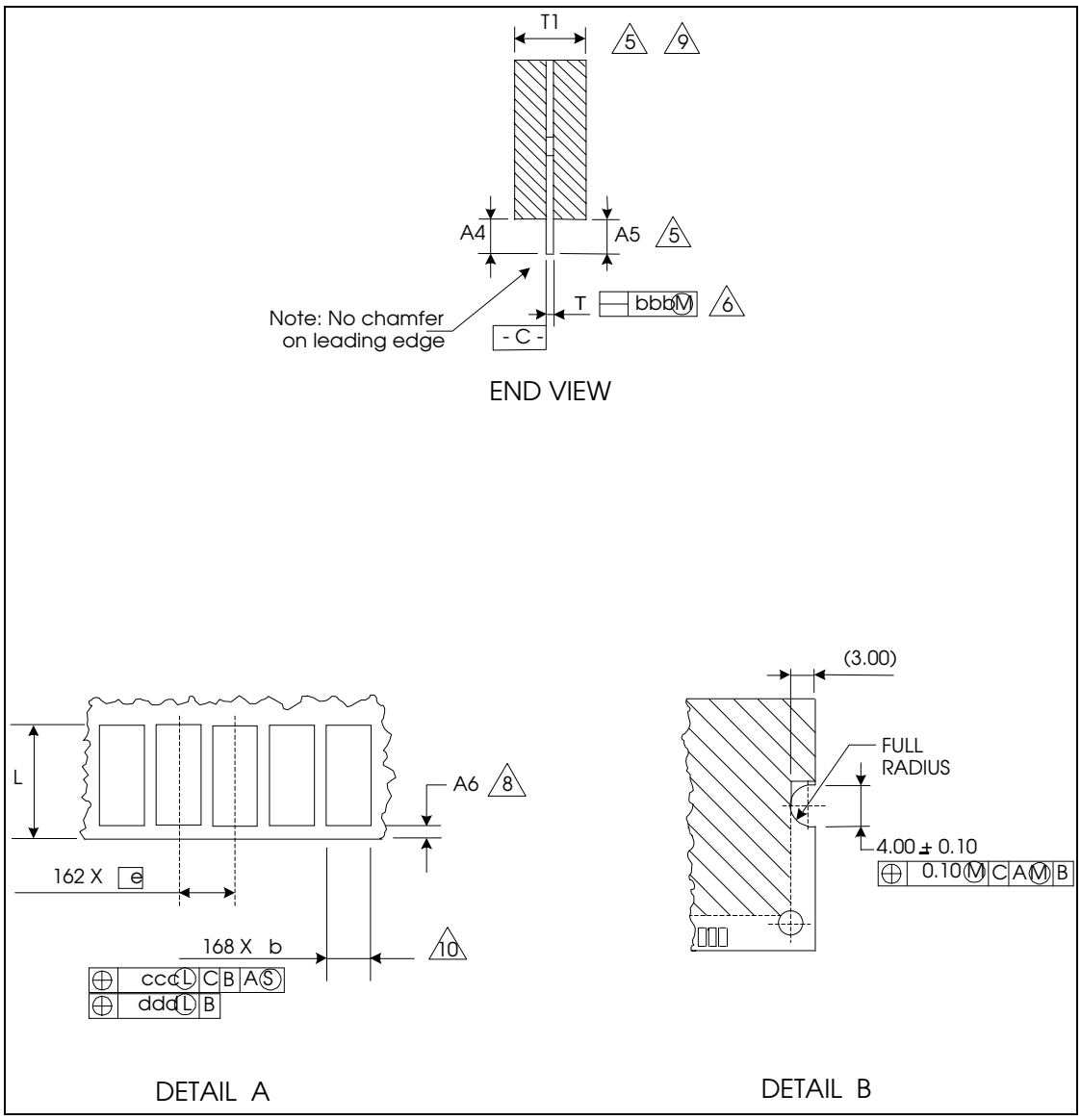


Figure 3: DIMM Mechanical Drawing (3 of 5)

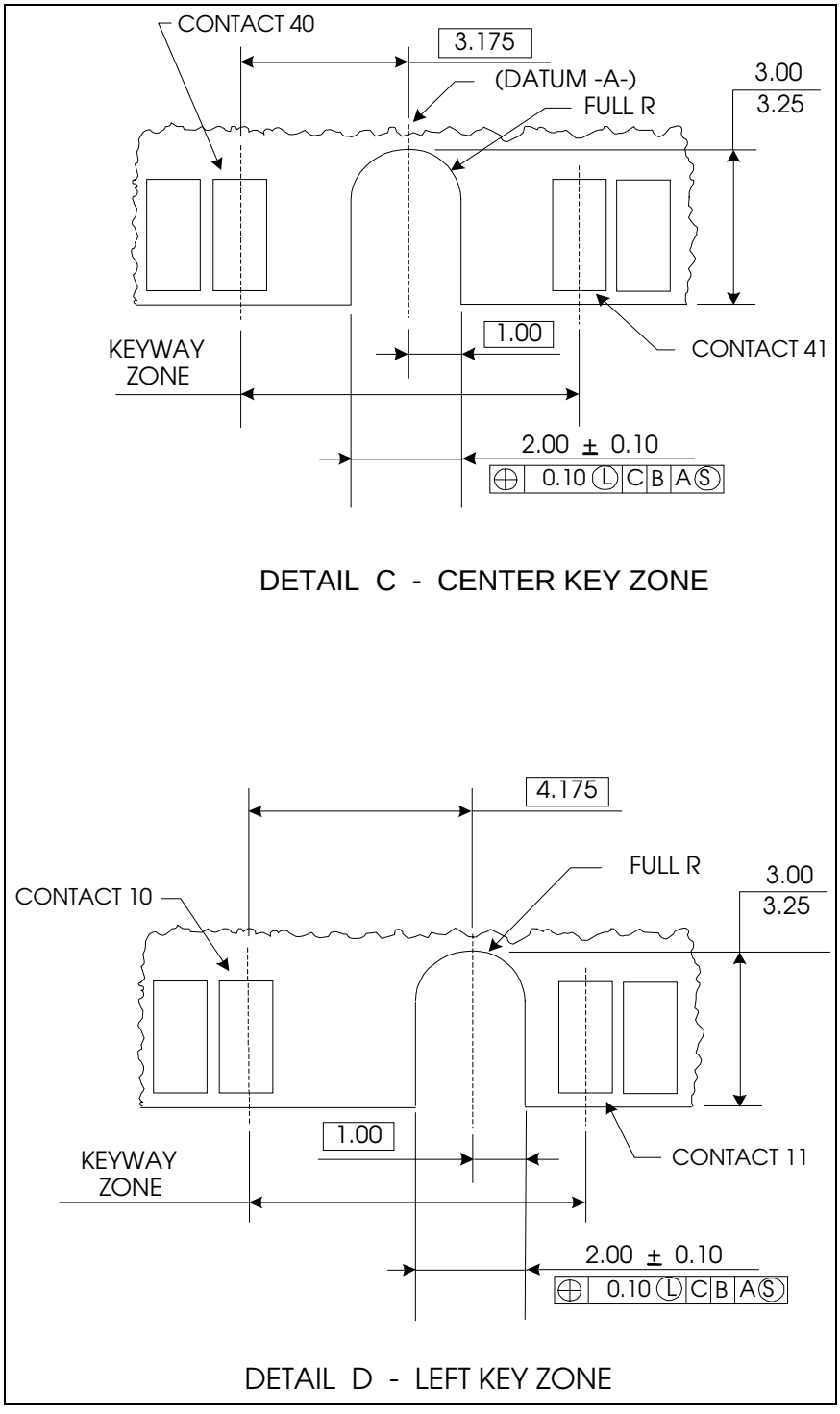


Figure 4: DIMM Mechanical Drawing (4 of 5)

NOTES

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-

2 TOLERANCES ON ALL DIMENSIONS +/- 0.13 UNLESS OTHERWISE

3 ALL DIMENSIONS ARE IN MILLIMETERS.

4 3.00 mm TYPICAL APPLIES TO BOTH 4.00 mm WIDE NOTCH LENGTH AND COMPONENT KEEPOUT AREA.

5 DIMENSION APPLICABLE WHEN COMPONENTS MOUNTED ON BOTH

6 CARD THICKNESS APPLIES ACROSS THE CONTACTS AND PLATING AND/OR METALIZATION. STRAIGHTNESS CALLOUT TO ZONE DEFINED BY A4, A5, AND D1.

7 N IS THE TOTAL NUMBER OF CIRCUIT CONTACTS (PINS, TABS OR PADS).

8 LEADING EDGE OF CONTACT ZONE SHALL BE FREE OF BURRS EXTERNAL TIE BARS.

9 THE MAXIMUM THICKNESS OVERALL SHALL NOT EXCEED 8.13 mm.

APPLICATION NOTES:

10 PLATING FOR CONTACT PADS: GOLD PLATING 0.75 MINIMUM OVER NI PLATING 2 MICROMETERS

11 FOR OPTIMUM PERFORMANCE, IT IS RECOMMENDED THAT THE BE OFFSET FROM THE CENTERLINE OF THE PAD. ALSO, THE TIEBAR MAY BE AN INTERNAL LAYER, SO THE REMNANT CANNOT CAUSE DAMAGE.

Figure 5: DIMM Mechanical Drawing (5 of 5)

4. Module Pins

The following table provides the 168-pin 72-bit registered DIMM module connector pinouts. Note that the eight error detection and correction bits CB(0:7) are actually NC for the 64-bit pinout.

Table 6: SDRAM DIMM pinout

Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name	Pin#	Signal Name
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	/S3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vcc	48	DU	90	Vcc	132	A13
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	Vref, NC	104	DQ47	146	Vref, NC
21	CB0	63	CKE1	105	CB4	147	REGE
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	/S0	72	DQ27	114	/S1	156	DQ59
31	DU	73	Vcc	115	/RAS	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10 (AP)	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	CK1	167	SA2
42	CK0	84	Vcc	126	A12	168	Vcc

Note: NC = Not Connected; DU = Don’t Use

Table 7: Pin Descriptions

CK(0:3)	Clock Inputs	DQ(0:63)	Data Input/Output
CKE(0:1)	Clock Enables	CB(0:7)	ECC Data Input/Output
/RAS	Row Address Strobe	DQMB(0:7)	Data Mask
/CAS	Column Address Strobe	Vcc	Power (3.3V)
/WE	Write Enable	Vss	Ground
/S(0:3)	Chip Selects	NC	No Connect
A(0:9,11:13)	Address Inputs	SCL	Serial Presence Detect Clock Input
A10/AP	Address Input/Autoprecharge	SDA	Serial Presence Detect Data Input/Output
BA0-BA1	SDRAM Bank Address	SA(0:2)	Serial Presence Detect Address Inputs
REGE	Register Enable	WP	Write Protect for SPD on DIMM
DU	Don't Use - leave as NC	NC	No Connect

All pin functions are described in the "Intel PC SDRAM Specification" with the exception of REGE.

REGE is the Register Enable pin which permits the DIMM to operate in "buffered" mode (inputs re-driven asynchronously) and "registered" mode (signals re-driven to SDRAMs when clock rises, and held valid until next rising clock). To conform to this specification, motherboards must pull this pin to a high state ("registered" mode).

5. SDRAM DIMM Block Diagrams

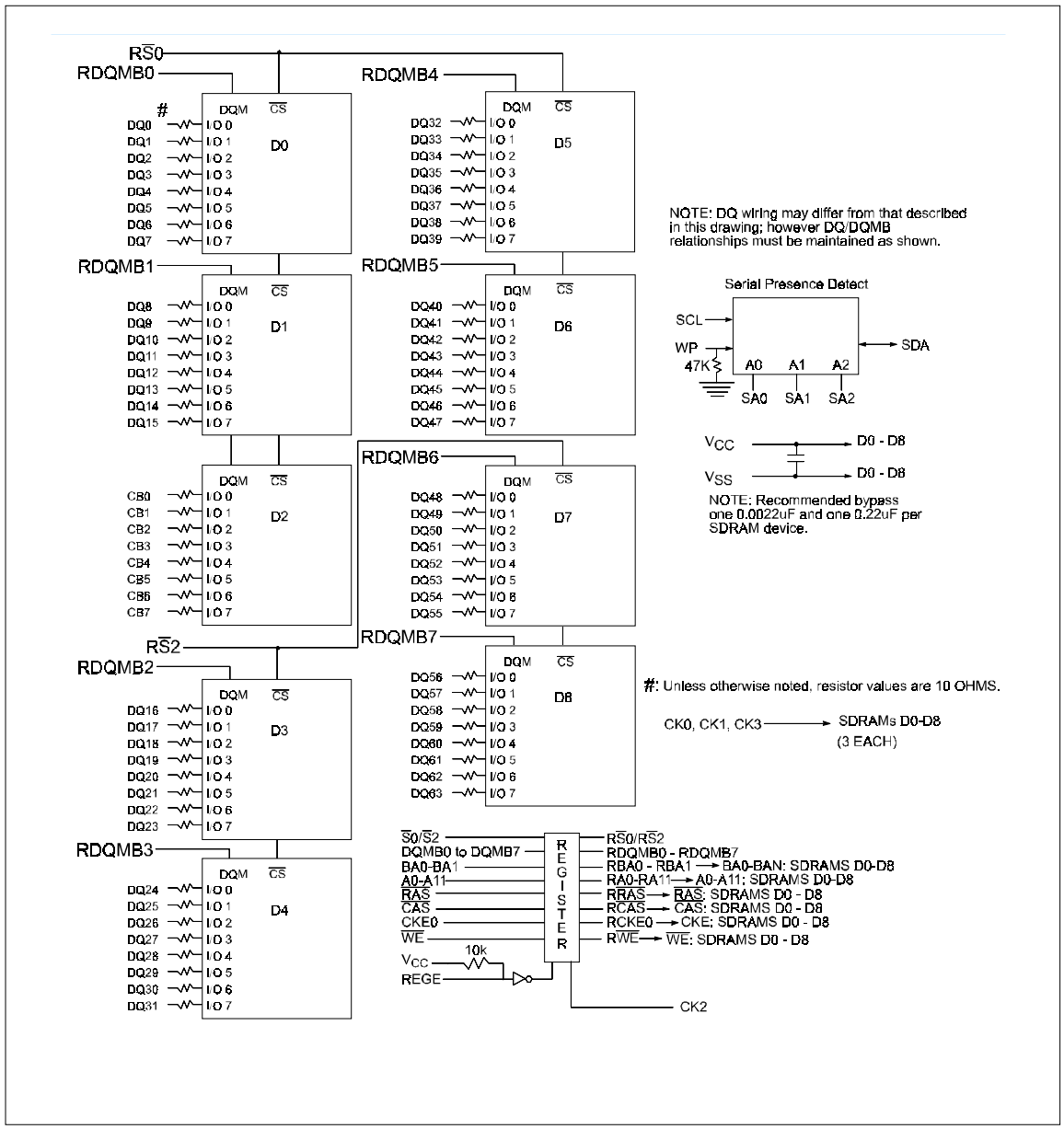


Figure 6: 64MByte 72-Bit ECC SDRAM DIMM Block Diagram (1 row x8 SDRAMs), non-PLL Implementation

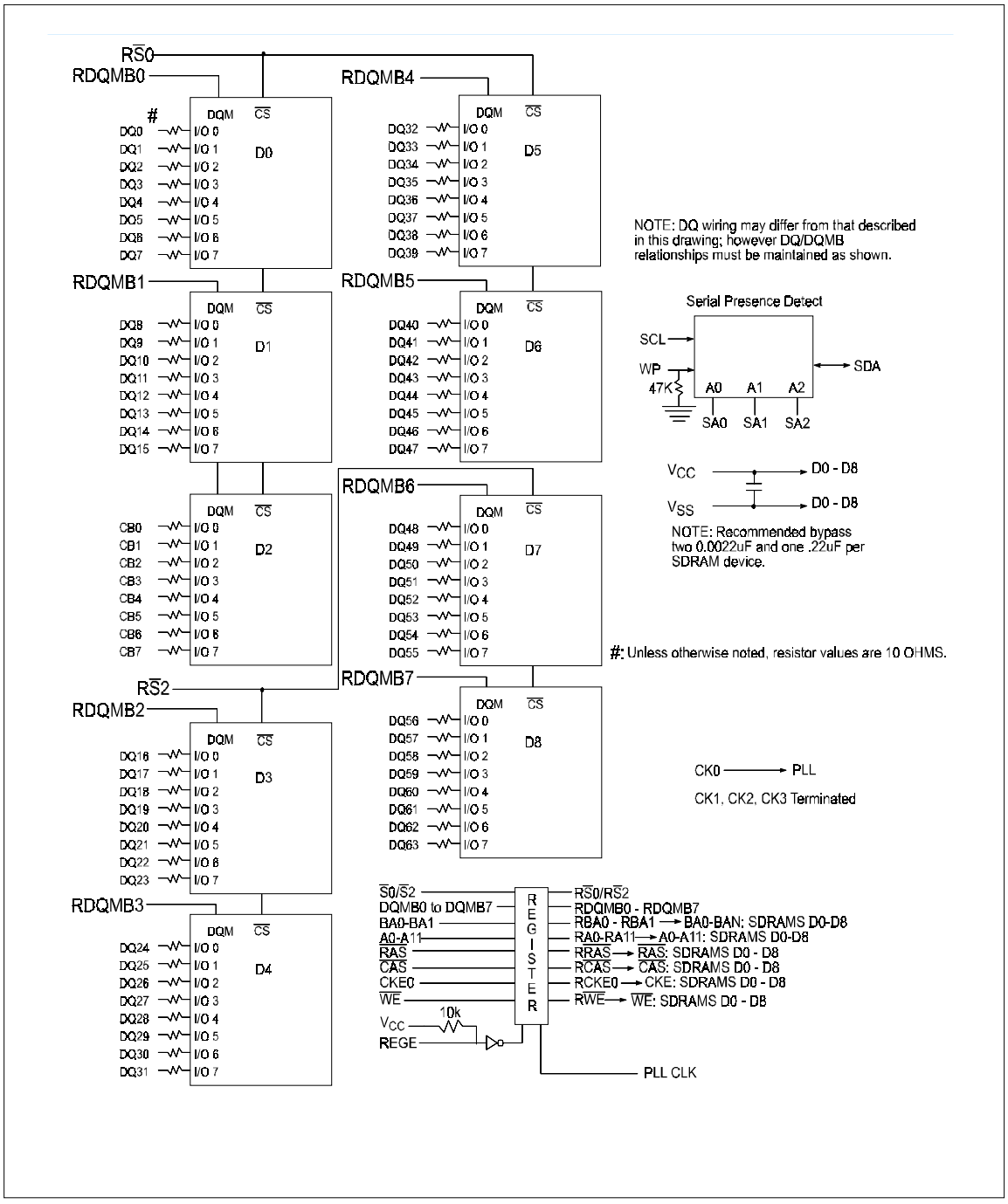


Figure 7: 64MByte 72-Bit ECC SDRAM DIMM Block Diagram (1 row x8 SDRAMs), PLL Implementation

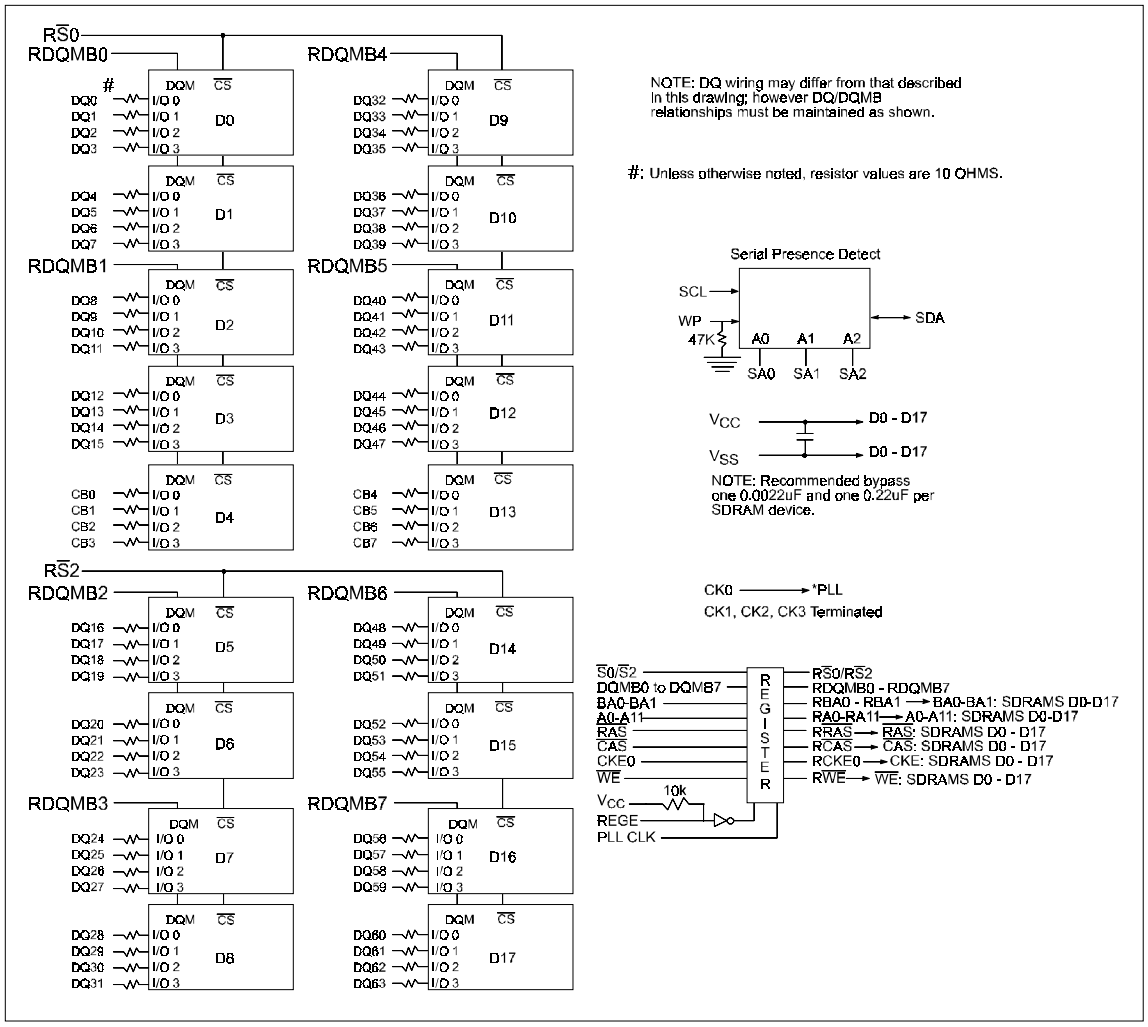


Figure 8: 128MByte 72-Bit ECC SDRAM DIMM Block Diagram (1 row x4 SDRAMs)

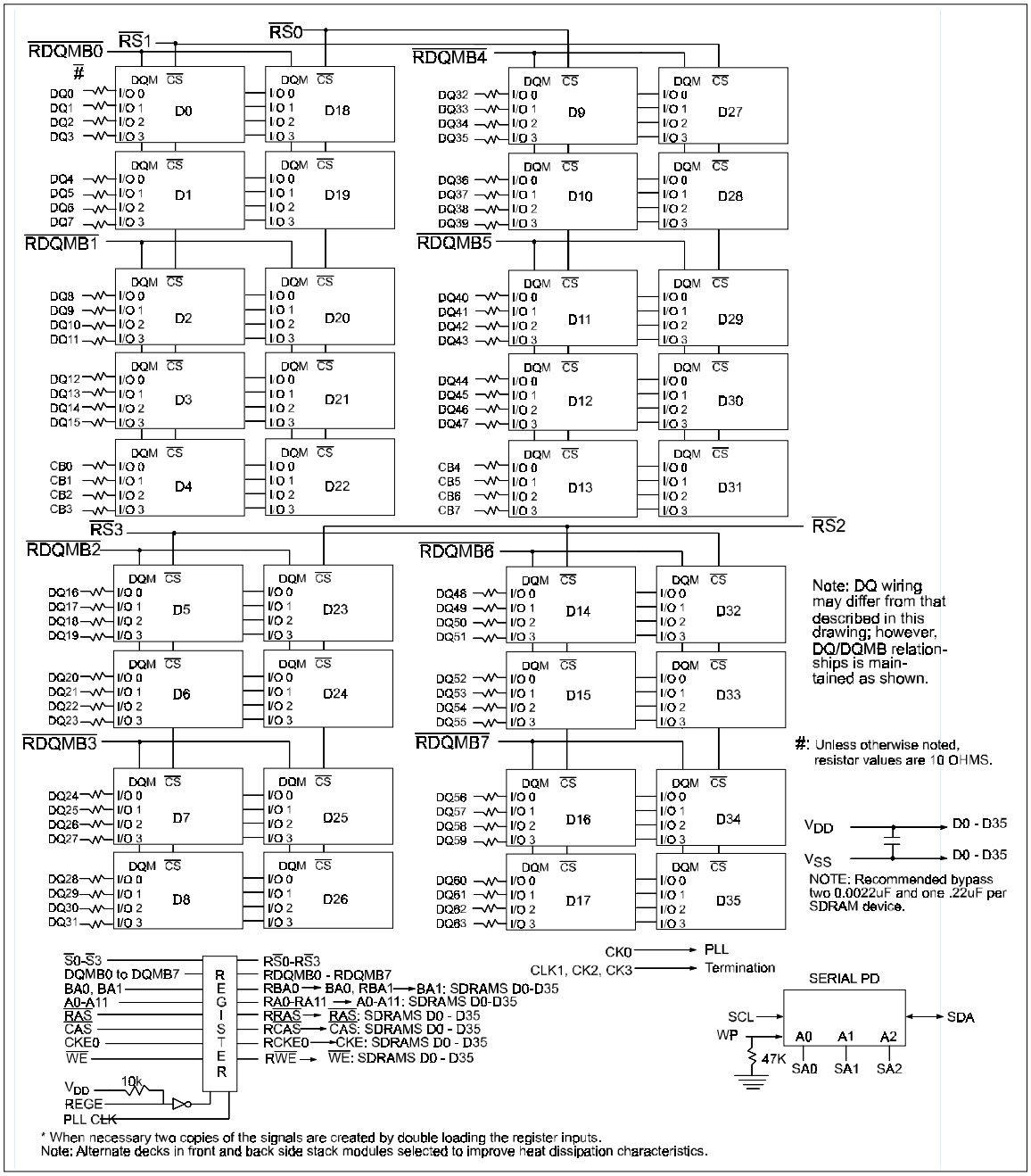


Figure 9: 72-Bit ECC SDRAM DIMM Block Diagram (2 rows x4 SDRAMs)

256MB using 16Mx4 (64Mbit) stacked SDRAM
512MB using 32Mx4 (128Mbit) stacked SDRAM

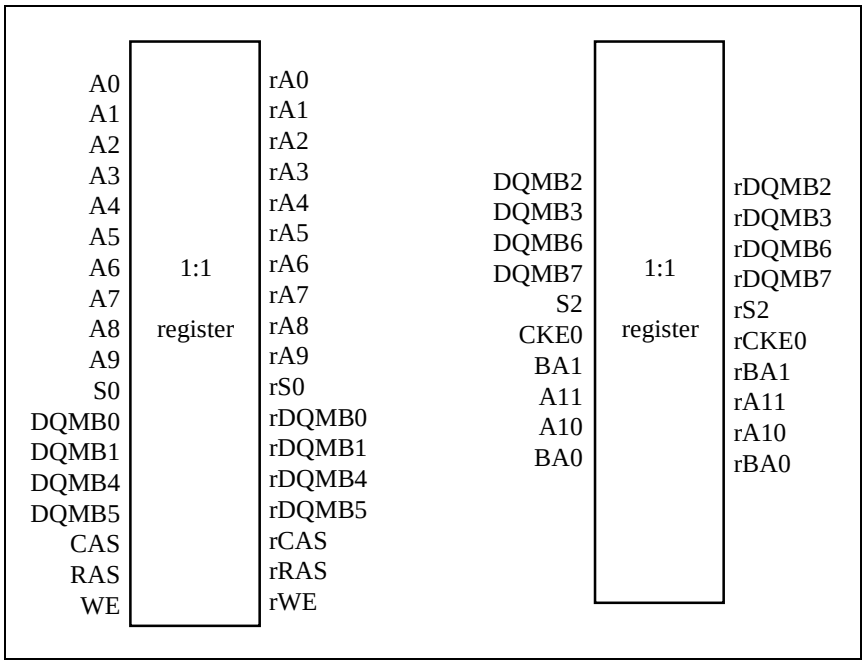


Figure 10: Register Wiring on 64MByte DIMMs

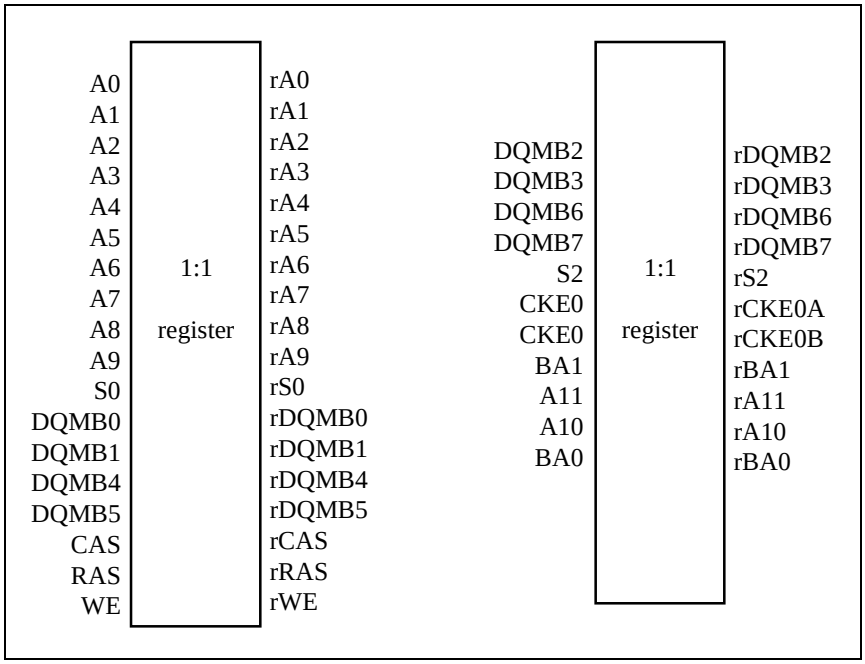


Figure 11: Register Wiring on 128MByte DIMM

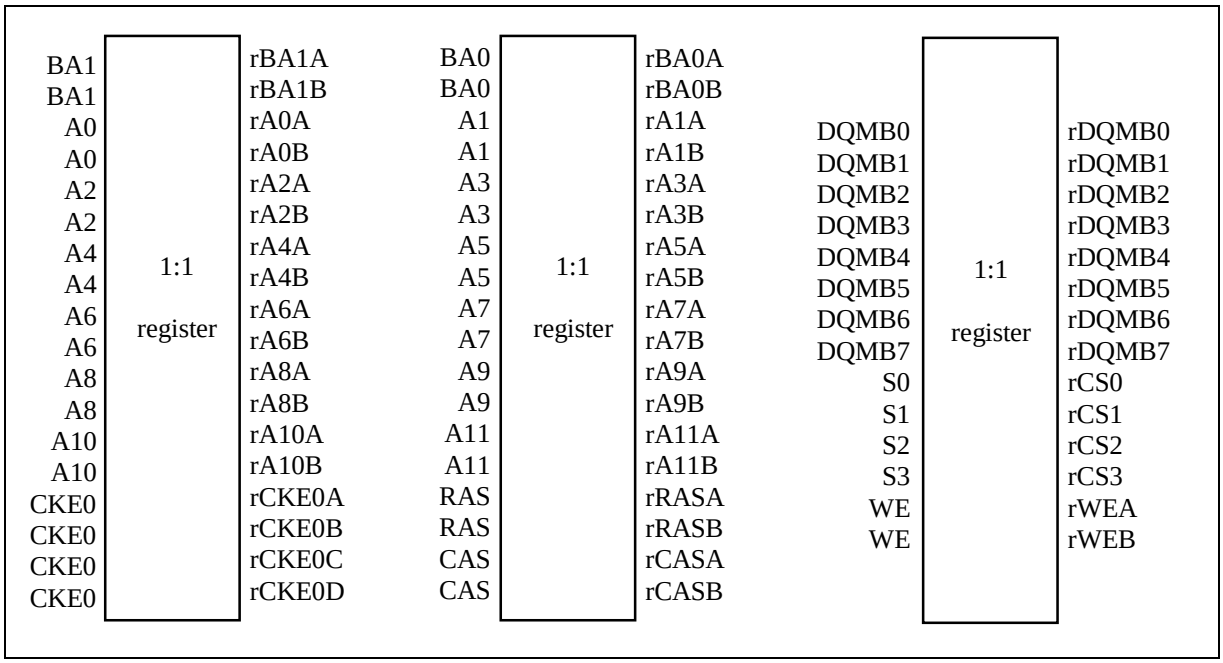


Figure 12: Register Wiring on 256MByte DIMM

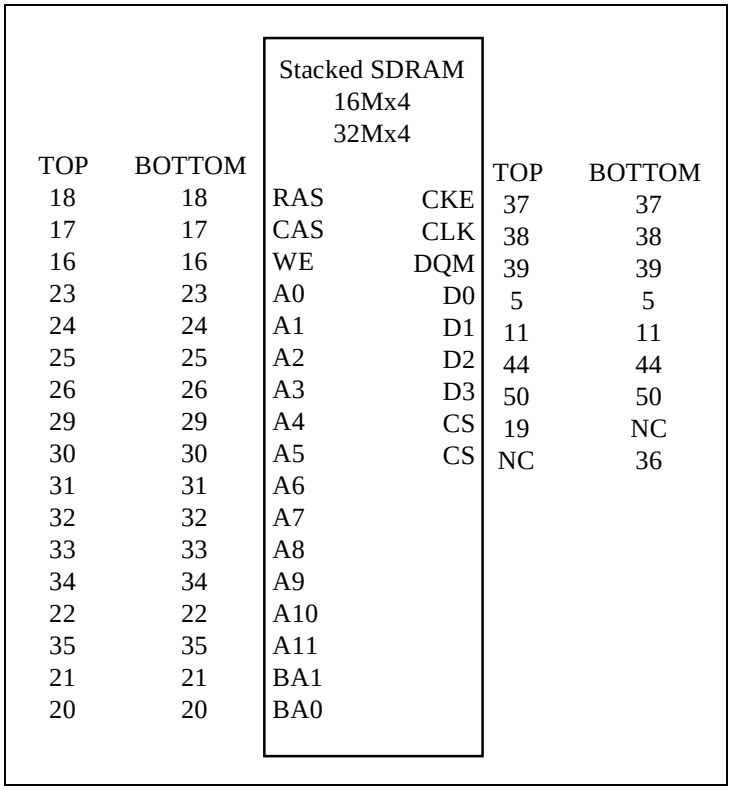


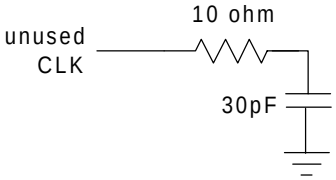
Figure 13: Stacked SDRAM Component Pinout

Clock Loading Table:

DIMM config	# of Banks on DIMM	Total # of SDRAMs	CLK Loading			
			CK0	CK1	CK2	CK3
64MB w/o PLL	1	9	SDRAM (3x)	SDRAM (3x)	Reg. (2x)	SDRAM (3x)
64MB w/PLL	1	9	PLL	*	*	*
128MB	1	18	PLL	*	*	*
256MB	2	36	PLL	*	*	*
512MB	2	36	PLL	*	*	*

* Use termination R/C

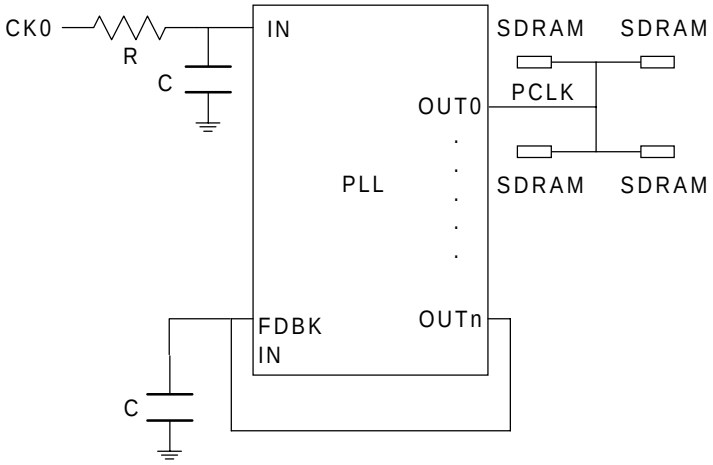
Termination R/C for CK signals not connected to SDRAMs:



NOTES:
1) PLL ouputs (PCLK) must be wired to assure tracking within +/- 100ps at the load (SDRAM, register or padding capacitor).

2) The skew of the clocks input clocks to the DIMM must be +/- 250ps as measured at the DIMM tabs. (This is a motherboard requirement added for clarification.)

Clock Net Wiring (CK0):



NOTES:
1) Only one PLL output is shown. Any additional PLL outputs will be wired in a similar manner.

2) Max of 4 SDRAM loads should be placed on each PLL output. If less than 4 loads - adjust line lengths to compensate for lighter loading.

Figure 14: Clock Loading Table & Wiring Diagram

6. DIMM Post-Register Timing

The post register timing on the registered DIMMs are very critical. An **example** of the timing analysis is shown below, this is an example only, and not to be used for all DIMMs:

Property	Time (ns) Set-up		Property	Time (ns) Hold
tco.REG.max	3.00		tco.REG.min	1.40
tflight.max	3.39		tflight.min	1.60
tsso.brd.max	0.10		tsso.brd.min	0.00
tskew	0.45		tskew	0.45
tjitter	0.65		tjitter	NA
tsu.DRAM	2.00		thold.DRAM	-1.00
Total	9.59		Total	1.55
Period	10.00		Period	NA
Margin	0.41		Margin	1.55
tskew.behind	0.10		tskew.behind	0.10
Margin	0.51		**Margin**	1.45

Tco.REG.max: The maximum time for the signal to exit the register. This is measured into a 0pF load.
Tflight.max: The maximum time for the signal to propagate from the register to the SDRAM.
Tss.brd.max: The time the flight time is extended due to cross talk from other signals.
Tskew: The skew of the input clocks to the register and the SDRAM.
Tjitter: The jitter of the input clocks to the register and the SDRAM.
Tsu.DRAM: The setup time required for the SDRAM inputs.
Tskew.behind: The input clocks to the registers and the SDRAM are purposely skewed to aid in the setup time of the signals into the SDRAM.

Tco.REG.min: The minimum time for the signal to exit the register. This is measured into a 0pF load.
Tflight.min: The minimum time for the signal to propagate from the register to the SDRAM.
Thold.DRAM: The hold time required for the SDRAM inputs.

7. DIMM PCB Layout and Signal Routing

Printed Circuit Board

The DIMM printed circuit board should be a six layer design using glass epoxy material. PCBs must have both a full ground plane layer and full power plane layer. The PCB stackup must be designed to achieve the following calculated board characteristics (using either 4 or 6 mil wide traces):

Table 8: PCB Calculated Parameters

Parameter	Min	Max
Trace velocity: S_0 [ns/ft] (outer layers)	1.6	2.2
Trace velocity: S_0 [ns/ft] (inner layers)	2.0	2.2
Trace impedance: Z_0 [Ω] (all layers)	55	75

Required Dielectric: 4.2 to 4.8

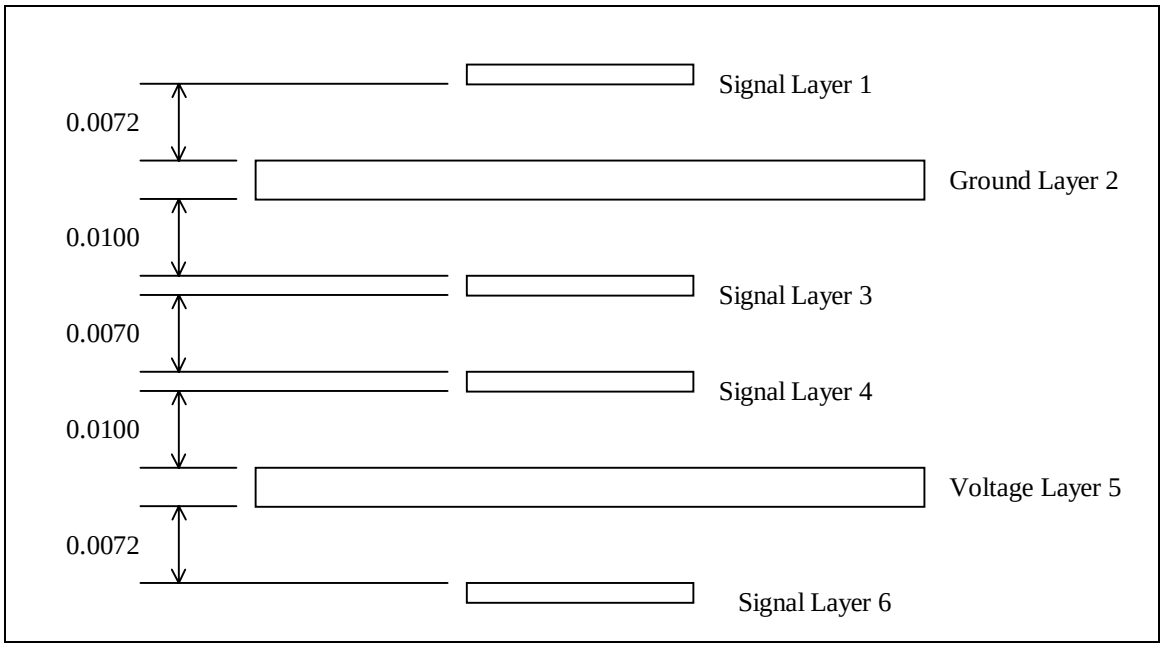


Figure 15: Example 6-Layer Stackup for 6 mil Traces

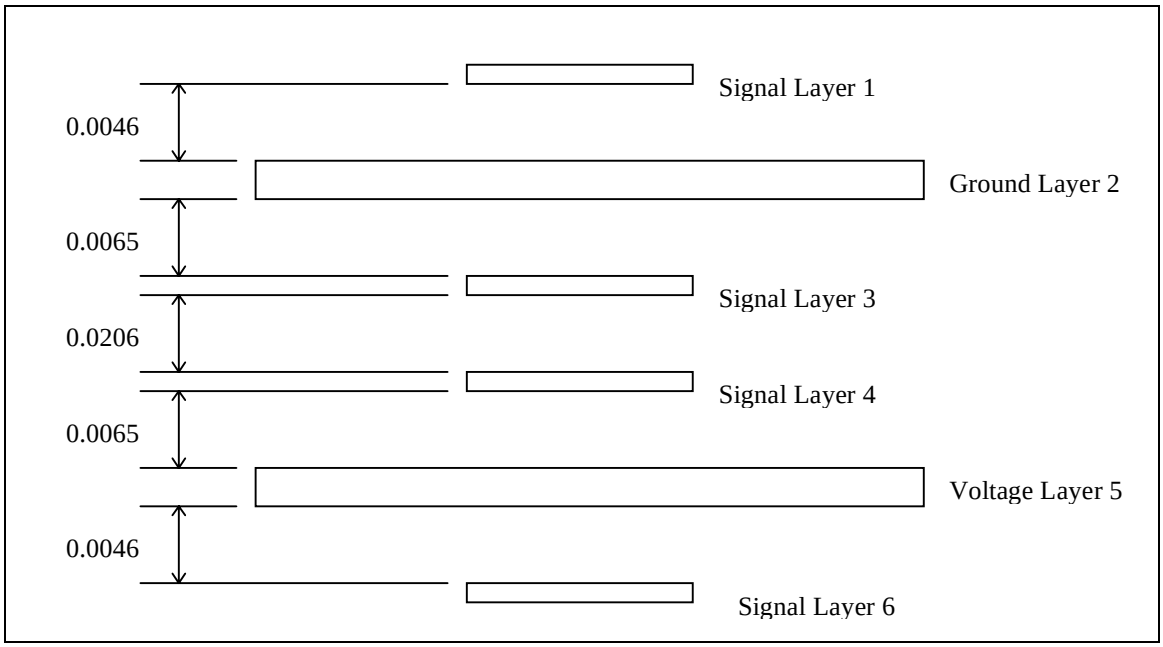


Figure 16: Example 6-Layer Stackup for 4 mil Traces

The PCB edge connector contacts shall be gold plated per Figure 5 note 10. Note: The PCB connector edge will not be chamfered.

Assembled DIMM Naming Convention

In order to be able to visually identify the critical parameters of a given DIMM, the following naming convention will be used.

On component or sticker on DIMM (supplier option):

PCX-abc-defR (use minimum 8point font)

Where X=Mhz
a = CL value
b = trcd value
c = trp value
d = tac value
e = spd rev #
f = reserved

Example: PC100-322-620R
is 100Mhz, CL3, trcd=2, trp=2, tac=6, 2= spd rev 1.2, 0= reserved, R=registered DIMM

The manufacturer's name and DIMM assembly part number shall also appear on the DIMM

Component Types and Placement

Components shall be of surface mount type, and will be mounted on both sides of the PCB. Components shall be positioned on the PCB to meet the min and max trace lengths required for SDRAM data signals. Bypass capacitors for SDRAM devices must be located as near as practical to the device power pins. In two bank SDRAM designs, location of the second SDRAM bank devices will be stacked on top of the first bank SDRAM devices.

The following diagram illustrates the suggested placement for x4 (stacked) SDRAM devices. Exact spacing numbers are not provided, but are left up to the DIMM manufacturer to determine based on manufacturing constraints and signal routing constraints imposed by this design guide.

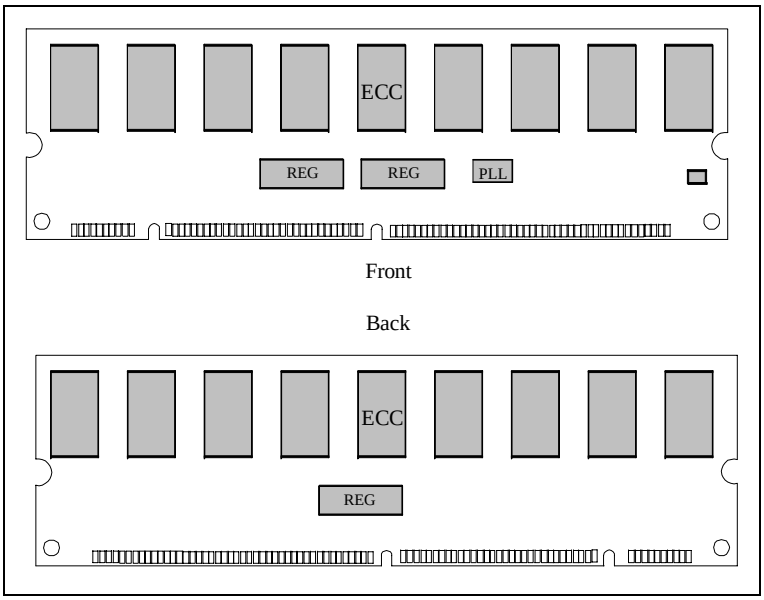


Figure 17: Example 256MByte Component Placement

Signal Groups

In this specification, the SDRAM timing-critical signals have been categorized into seven groups. The signals are divided into groups whose members have identical loadings and routing topologies. The following table summarizes the signal groups by listing the signals contained in each. The following sections will describe routing restrictions associated with each signal group.

Table 9: Signal Topology Categories

SIGNAL GROUP	SIGNALS IN GROUP
Clock	CK [3:0]
Data	DQ [63:0]
	CB [7:0]
Data Mask	DQMB [0,2-4,6,7]
Data Mask	DQMB [1,5]
Chip Select	CS# [3:0]
Clock Enable	CKE# [0]
Address/Control	A [12:0]
	BA [0,1]
	RAS#
	CAS#
	WE#

Signal Topology and Length Restrictions

In order to meet signal quality and setup/hold time requirements for the memory interface certain routing topologies and trace length requirements must be met. The signal topology requirements are shown pictorially in the following pages. Each topology diagram is accompanied by a trace length table that lists either the minimum and maximum lengths allowed for each trace segment or the min and max lengths for the entire net.

Routing Rules

General Info: All signal traces except clocks are routed using either 6/10 or 4/6 rules.
(6 mil traces and 10 mil minimum spacing between adjacent traces).

Clocks should be done in 6 mil trace width and 12 mil minimum spacing, or 4 mil trace width and 18 mil spacing.

Clocks must be routed with at least 90% of the total trace length in the inner layers.

No test points are required.

Topology Diagram Explanation and Examples

A reference design example is documented in this specification. The reference design is intended to provide an initial basis for a registered DIMM design. For any design, a full simulation of all signal integrity and timing is required to verify the functionality of the DIMM. The following topologies are a representation of the reference design, and are not meant to be inclusive for all solutions.

The routing topology diagrams in this section should be used to determine individual signal topologies on a DIMM for any supported configuration.

The way that these diagrams should be read is the following:

> Only the cylinders labeled with length designators represent actual physical trace segments. All other lines should be considered zero in length.

Please see the following page for an example of how to use the topology diagrams.

**** With the exception of the clock topologies, all references to 64MByte DIMM topologies refer to both the PLL and non-PLL versions of the DIMMs.**

Example: For an 256MByte, double-sided, ECC DIMM that uses 64Mbit 16Mx4 SDRAM devices, the resulting topology for Data, would be the following:

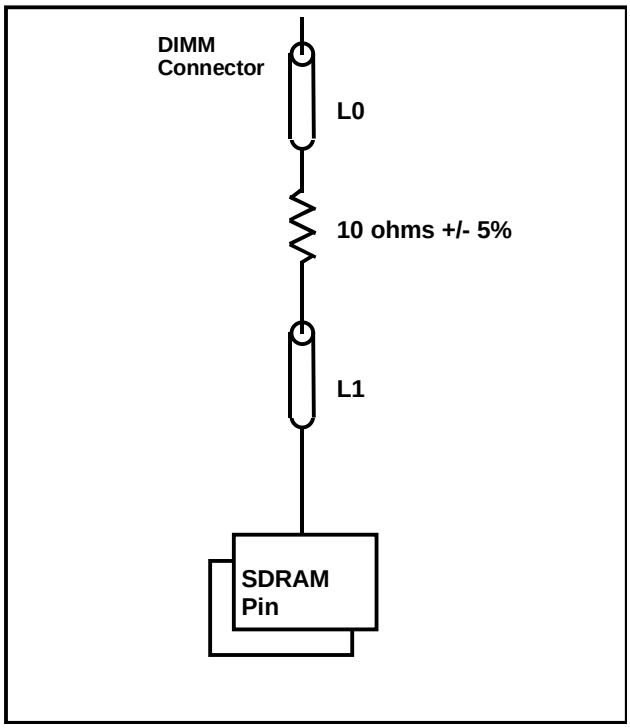


Figure 18: Example Topology

Once the topology has been determined, the permitted segment length ranges for that topology can be read from the table below each topology diagram. It is important to note that some configurations will require more than one topology diagram to account for different numbers of loads on copies of the same signal. For all of the topologies listed in the following pages, one load is defined as one SDRAM input.

Topology for Clock: CK[3:0]

Special attention must be given to the routing of the SDRAM clock signal(s) to ensure adequate signal quality, rise/fall time, minimum skew between clock edges at each SDRAM component, and predictable skew to motherboard chipset clocks. The clocks must be matched to minimize skew, and the trace lengths and loads must be chosen to match the delays of an unbuffered DIMM.

Clocks must be routed with at least 90% trace length in the inner layers. The following figure illustrates the recommended clock topologies, and the accompanying table lists required trace segment lengths and added capacitance values and tolerances.

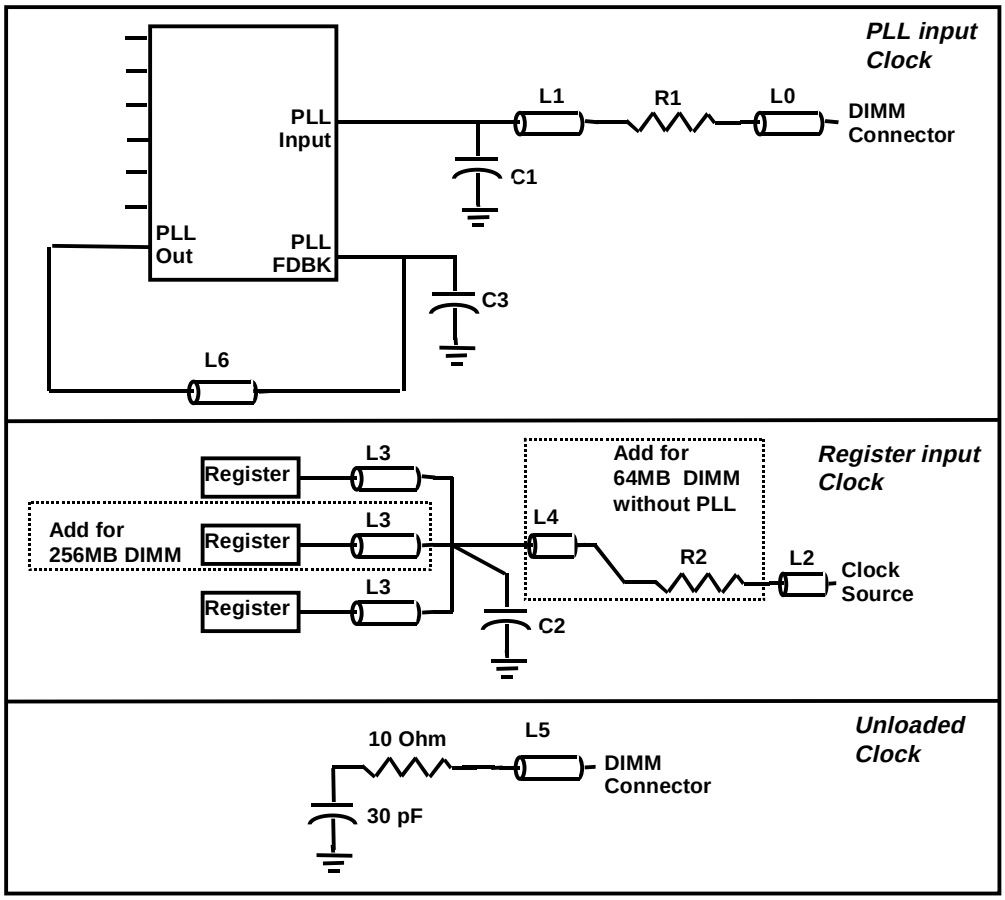


Figure 19: Signal routing topologies for Clocks pre-PLL

Table 10: Trace Length Table for pre-PLL Clock Topologies

DIMM Config	L0	L1	L2	L3	L4	L5	L6	R1 ohms	R2 ohms	C1 pF	C2 pF	C3 pF
64MB*	0.178	1.785	1.645	2.500	NA	0.150	3.000	10	NA	24	NA	12
64MB	NA	NA	0.141	0.757	2.472	NA	NA	NA	25.5	NA	2.7	NA
128MB	0.275	2.410	1.311	0.381	NA	0.214	2.000	10	NA	NA	NA	NA
256MB	0.126	2.637	1.096	0.850	NA	0.145	3.102	10	NA	27	NA	27

1 All distances are given in inches and must be kept within a tolerance of +/- 0.01 inches
2 All capacitances are given in picoFarads and must be kept within a tolerance of +/- 5%
* 64MB with PLL

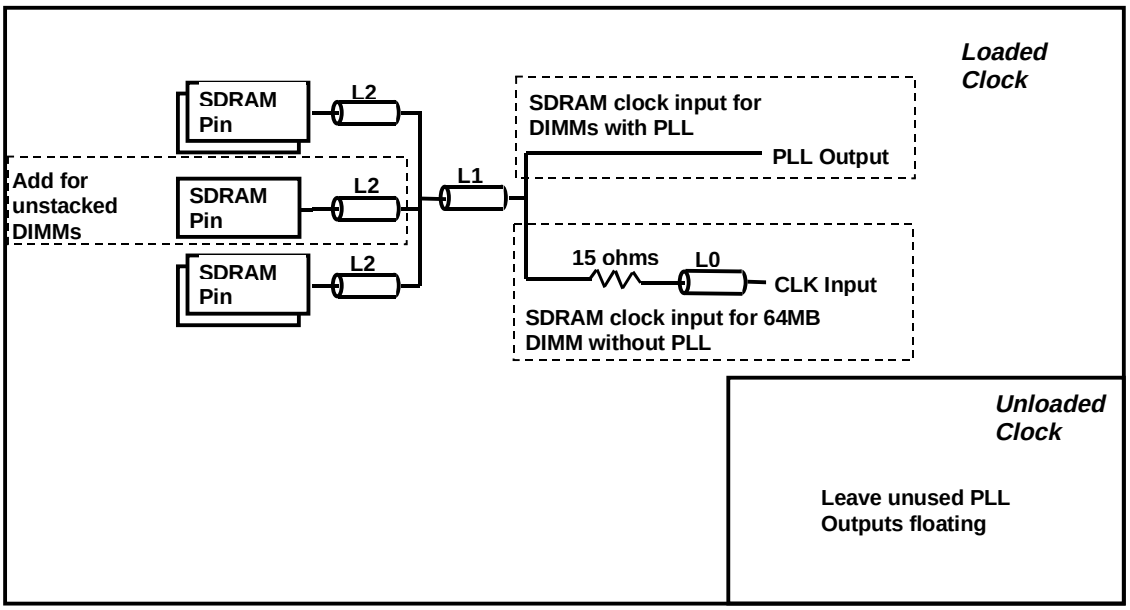


Figure 20: Signal routing topologies for Clocks post-PLL

Table 11: Trace Length Table for Clock Topologies

DIMM Config	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2	Total Length
64MB*	3	NA	NA	1.856	1.860	1.270	3.128
64MB	3	0.134	0.189	1.901	1.957	1.270	3.361
128MB	3	NA	NA	3.079	3.082	0.375	3.455
256MB	4	NA	NA	3.444	3.446	0.200	3.645

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches
2 All capacitances are given in picoFarads and should be kept within a tolerance of +/- 5%
* 64MB with PLL

Topology for Data: DQ[63:0] & CB[7:0]

The table defines the line length ranges allowed for these signals. For the purpose of specifying trace segment lengths, the data lines have been broken down into two subcategories based on the location of their edge connector pins. These two data "zones" have lengths specified that make the data lines connecting toward the outside edge shorter in min and max length. This is done to allow the opportunity to pair the necessarily longer data line traces on the motherboard with traces that can be made shorter on the DIMMs, and the necessarily longer DIMM traces with the potentially shorter traces on the motherboard.

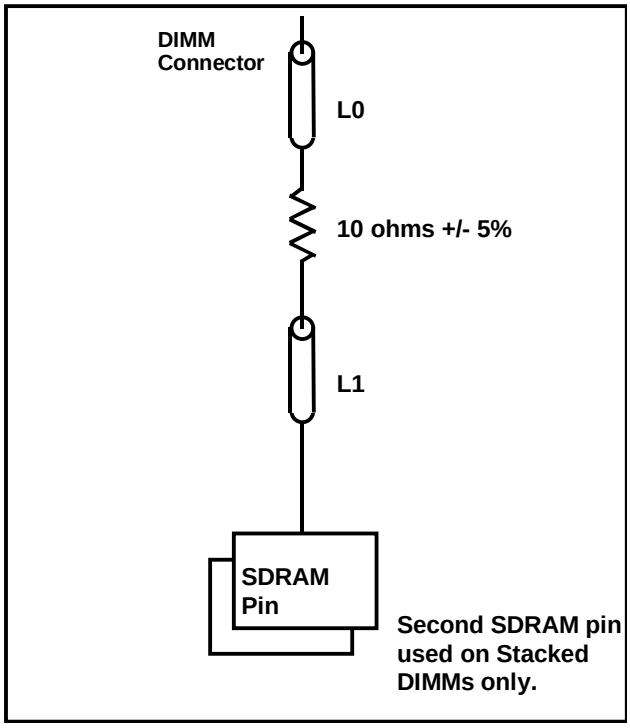


Figure 21: Signal routing topologies for Data

Data Zone I : DQ [63-56, 39-24, 7-0]
Data Zone II : DQ [55-40, 23-8] ; CB [7-0]

Table 12: Trace Length Table for Data Topologies

DIMM Size	# of loads	Zone	L0 Min	L0 Max	L1 Min	L1 Max	Total Min	Total Max
64MB	1	I	0.126	0.154	0.834	0.861	0.982	1.000
64MB	1	II	0.127	0.163	0.850	1.000	1.000	1.249
128MB	1	I	0.126	0.153	0.950	0.952	1.076	1.103
128MB	1	II	0.126	0.162	1.210	1.542	1.338	1.675
256MB	2	I	0.127	0.148	0.973	1.048	1.115	1.183
256MB	2	II	0.126	0.345	1.139	1.518	1.424	1.702

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches
2 Total Min and Total Max refer to the min and max respectively of L0 + L1.

Topology for Data Mask (1/2/4 Loads): DQMB[7,6,4-2,0]

These signals are routed using a " Y" topology on any layer. The tables define the line length ranges allowed for these signals.

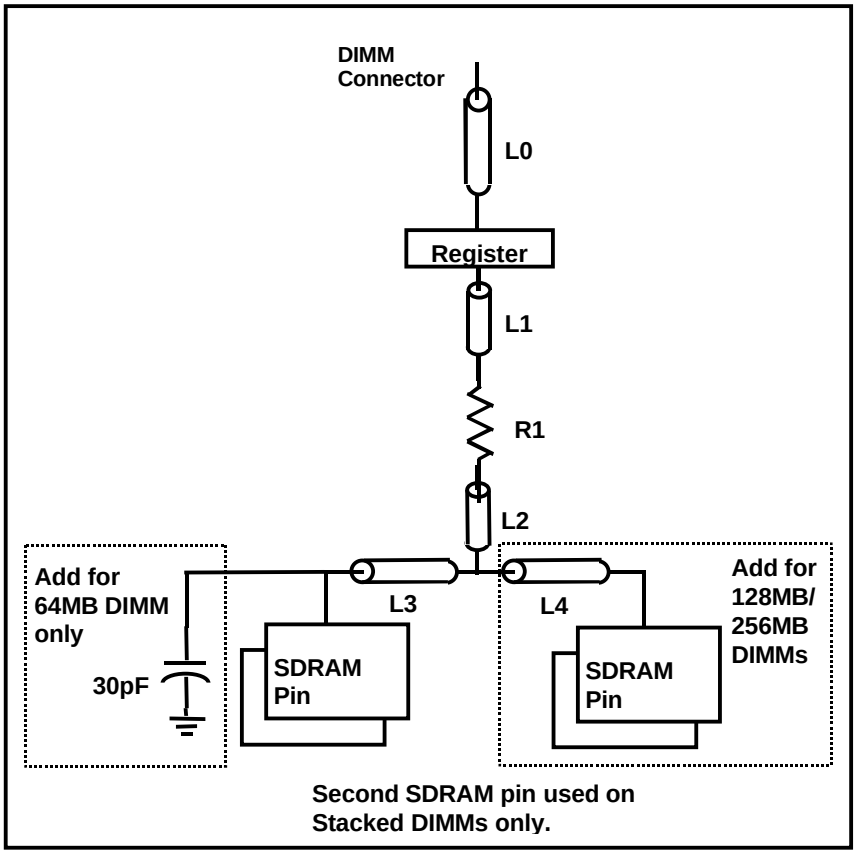


Figure 22: Signal routing topologies for Data Mask (1/2/4 Loads)

Table 13: Trace Length Table for Data Mask Topologies (2/4 Loads)

DIMM config	# Loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	L4 Min	L4 Max	Total Min	Total Max	R1 ohms
64MB	1	0.268	0.343	0.113	0.167	0.799	1.702	0	--	NA	NA	1.274	2.109	33
128MB	2	0.219	0.539	0.138	0.174	3.185	4.229	0.304	--	0.524	--	3.862	5.339	75
256MB	4	0.190	1.219	0.111	0.266	2.844	3.202	0.238	--	0.470	--	3.563	4.756	10

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

Topology for Data Mask (3/6 Loads): DQMB[5,1]

These signals are routed using a star topology on any layer. The tables define the line length ranges allowed for these signals.

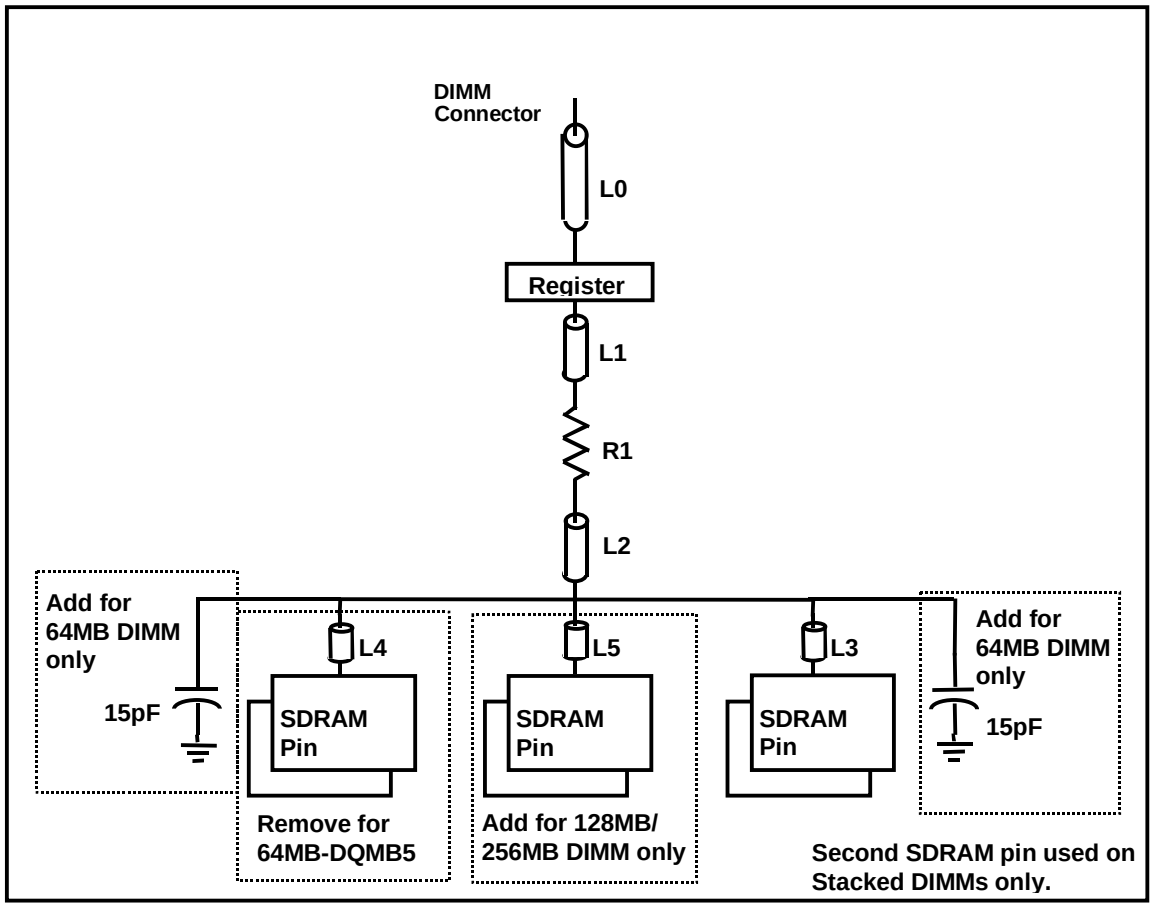


Figure 23: Signal routing topologies for Data Mask (3/6 Loads)

Table 14: Trace Length Table for Data Mask Topologies (1/2/3/6 Loads)

DIMM config	# Loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	L4 Min	L4 Max	L5 Min	L5 Max	R1 ohms
64MB	1-2	0.333	--	0.127	--	0.060	--	0.800	--	1.087	--	NA	NA	24.9
128MB	3	0.214	0.233	0.135	0.141	3.723	3.730	0.584	0.657	0.584	0.657	0.056	0.061	75
256MB	6	1.098	1.219	0.111	0.139	2.576	2.662	0.441	0.705	0.441	0.705	0.441	0.705	10

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

Topology for Chip Select: CS#[3:0]

This signal is routed using a balanced "comb" topology on any layer. The table below defines the line length ranges allowed for these signals. Once each segment length is decided upon, the other traces with the same length designator must lie within +/-10% of that length. For example, if L2 to one device is 500 mils, then L2 to all other devices must fall within 450 to 550 mils.

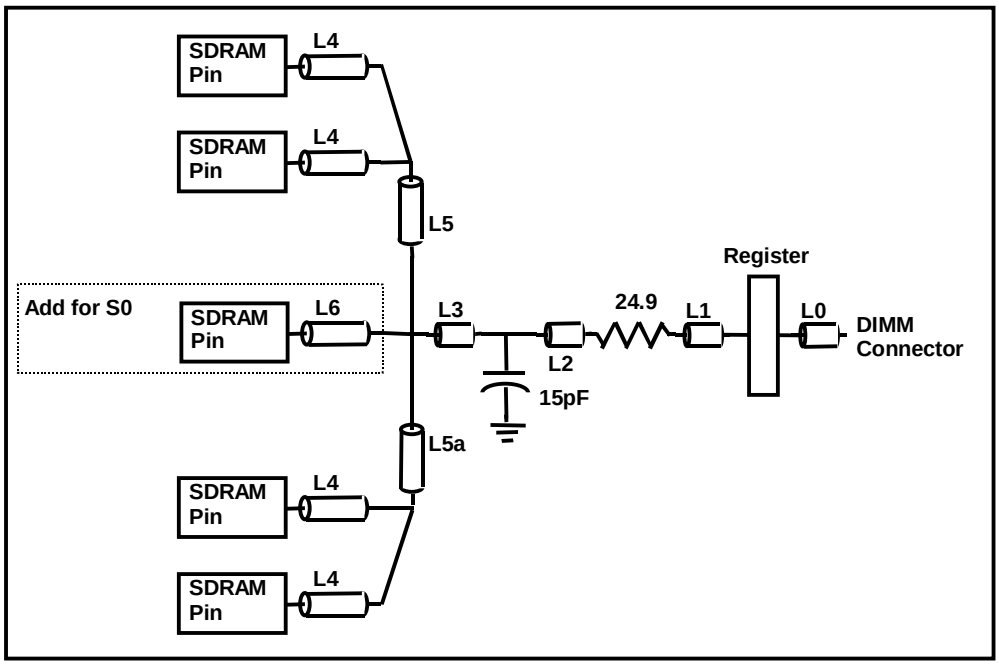


Figure 24: Signal routing topologies for Chip Select (64MB)

Table 15: Trace Length Table for Chip Select Topologies (S0, S1)

Comp Width	# of loads	L0	L1	L2	L3	L4 Min	L4 Max	L5	L5a	L6
64MB	5 S0	0.329	0.124	0.402	0.657	0.134	0.350	0.684	0	1.313
64MB	4 S2	0.276	0.124	1.187	0.370	0.134	0.350	0.238	0.443	NA

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

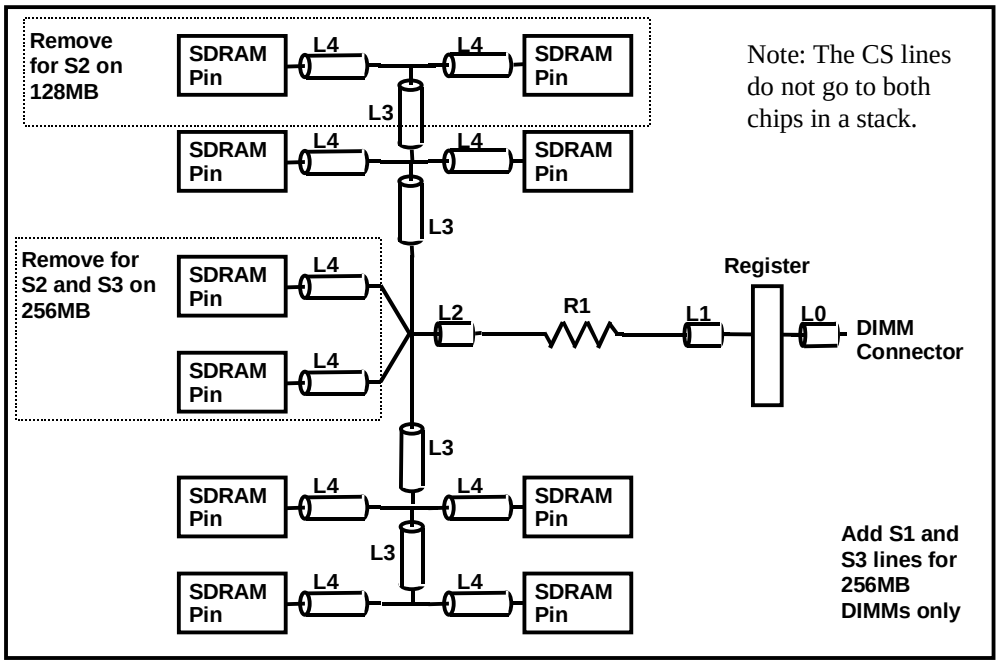


Figure 25: Signal routing topologies for Chip Select (128MB, 256MB)

Table 16: Trace Length for Chip Select Topologies (S0, S1, S2, S3)

Comp Width	# of loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	L4 Min	L4 Max	R1 Ohm
128MB	10 S0	0.293	--	0.122	--	1.960	--	0.557	0.629	0.221	0.257	60.4
128MB	8 S2	0.478	--	0.134	--	3.086	--	0.530	0.742	0.123	0.370	60.4
256MB	10 S0,S1	1.040	1.208	0.186	0.229	1.694	1.903	0.430	0.674	0.077	0.208	10
256MB	8 S2,S3	0.213	0.235	0.150	0.180	2.028	2.032	0.175	0.595	0.092	0.106	10

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

Topology for Clock Enable: CKE#[0]

This signal is routed using a balanced "comb" topology on any layer. The table below defines the line length ranges allowed for each trace segment.

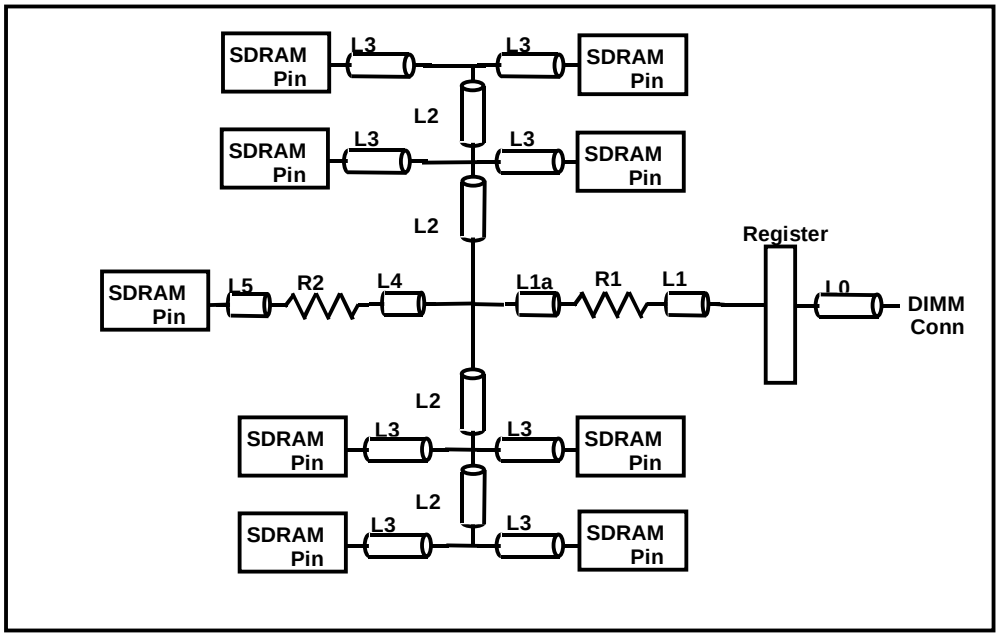


Figure 26: Signal routing topologies for Clock Enable (64MB)

Table 17: Trace Length Table for Address and Control Signals

DIMM config	# loads	L0 Min	L0 Max	L1 Min	L1 Max	L1a Min	L1a Max	L2 Min	L2 Max	L3 Min	L3 Max
64MB	9	0.289	0.686	0.110	0.172	0.576	1.212	0.661	1.401	0.125	0.375

DIMM config	L4 Min	L4 Max	L5 Min	L5 Max	R1 ohms	R2 ohms
64MB	0.058	0.181	0.127	0.272	0	100

1. All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

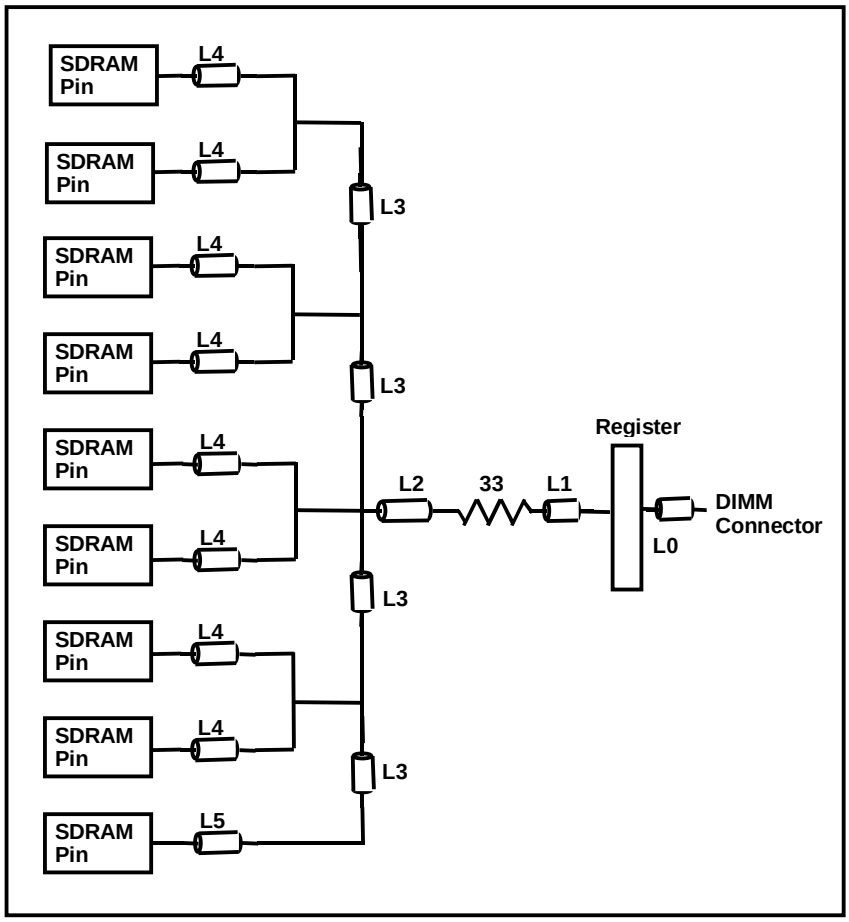


Figure 27: Signal routing topologies for Clock Enable (128MB)

Table 18: Trace Length Tables for Clock Enable Topologies

DIMM config	# Loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	L4 Min	L4 Max	L5 Min	L5 Max
128MB	9	0.138	--	0.149	0.313	2.045	2.983	0.365	0.711	0.185	0.317	0.069	0.105

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

Note: The CKE0 line is double loaded before the register, so the above diagram is repeated twice to route the CKE0 line to all 18 SDRAM.

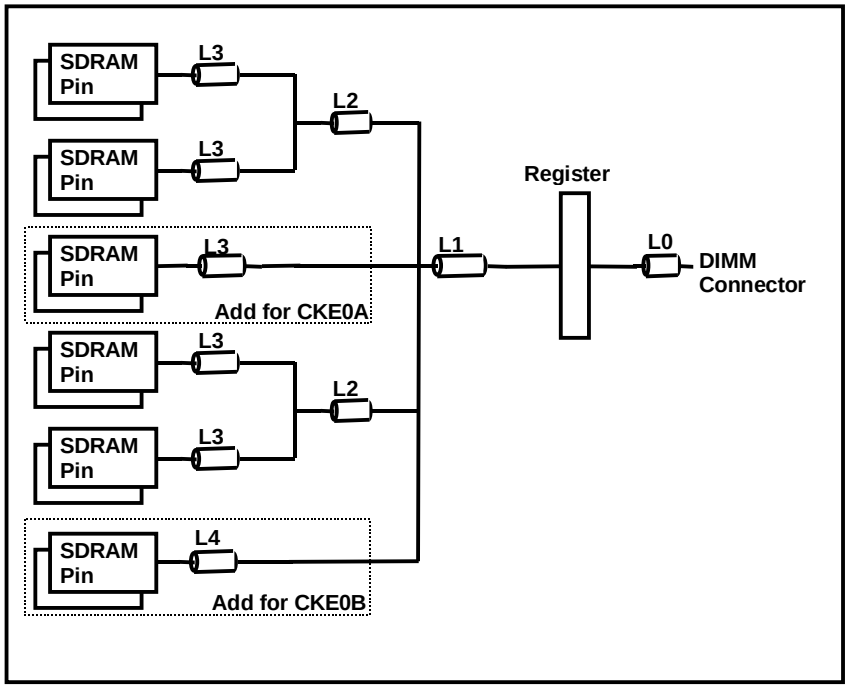


Figure 28: Signal routing topologies for Clock Enable (256MB)

Note: The CKE signal is routed to 4 register inputs, and the above topology is repeated 4 times (A-D).

Table 19: Trace Length Tables for Clock Enable Topologies

DIMM config	# Loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	L4
256MB	8-10	0.753	0.968	2.579	3.261	0.172	0.563	0.084	0.323	0.464

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

Note: The controller will need to drive both Chip Selects along with CKE0 simultaneously to place the 256MB DIMM in self refresh.

Address/Control: MAx, BAx, SRAS#, SCAS#, WE#(*)

These signals are routed using a balanced, double-sided "comb" topology on any layer. The table below defines the line length ranges allowed for these signals.

(*) topology applies to WE# for 64MB and 128MB designs.

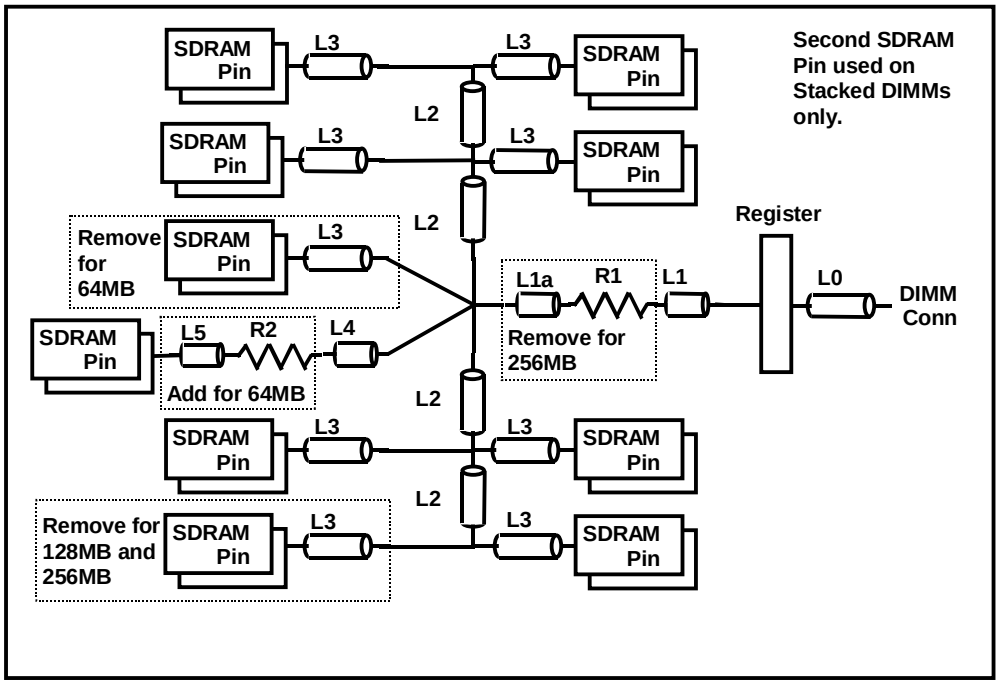


Figure 29: Signal routing topologies for Address and Control Signals

Note: The above signals are double loaded on the input to the register, so the above topology is repeated twice for the 256MB DIMM.

Table 20: Trace Length Table for Address and Control Signals

DIMM config	# loads	L0 Min	L0 Max	L1 Min	L1 Max	L1a Min	L1a Max	L2 Min	L2 Max	L3 Min	L3 Max	L4 Min	L4 Max	L5 Min	L5 Max
64MB	9	0.289	0.686	0.110	0.172	0.576	1.212	0.661	1.401	0.125	0.375	0.058	0.181	0.127	0.272
128MB	18	0.138	0.242	0.149	0.313	1.857	2.983	0.335	0.758	0.069	0.358	0.155	0.358	NA	NA
256MB	36	0.255	0.534	2.011	2.930	NA	NA	0.475	0.664	0.093	0.347	0.093	0.347	NA	NA

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

DIMM config	R1	R2
64MB	0	100
128MB	33	NA
256MB	NA	NA

256MB WE# Topology:

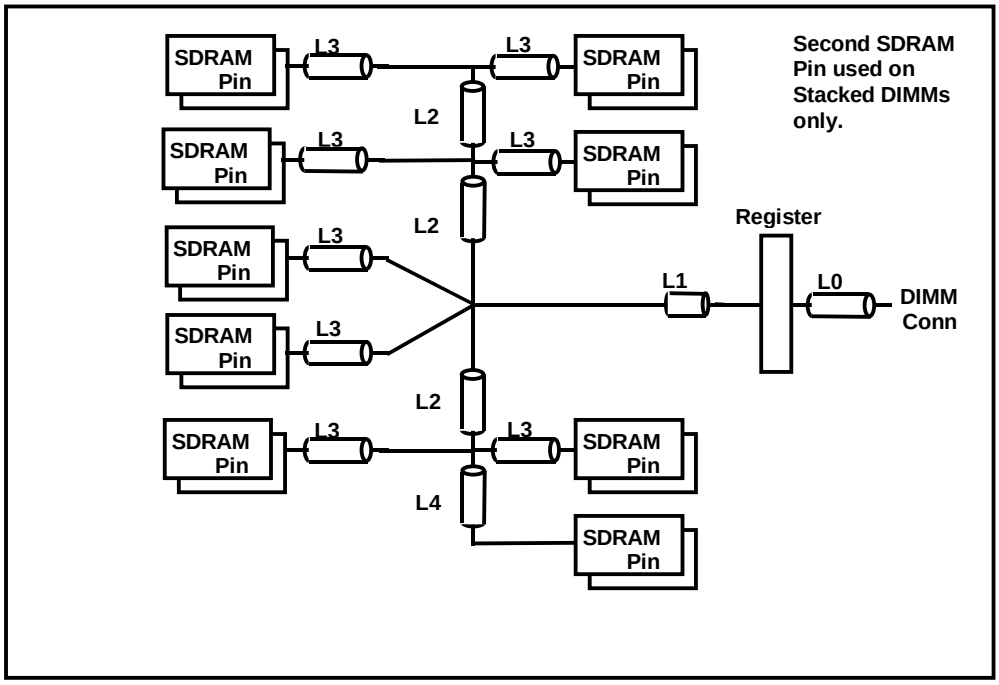


Figure 30: Signal routing topologies for Write Enable (256MB)

Note: The above signals are double loaded on the input to the register, so the above topology is repeated twice for the 256MB DIMM.

Table 21: Trace Length Table for Write Enable

DIMM config	# loads	L0 Min	L0 Max	L1 Min	L1 Max	L2 Min	L2 Max	L3 Min	L3 Max	L4 Min	L4 Max
256MB	36	1.255	1.255	1.943	1.943	0.255	0.501	0.076	0.252	0.768	0.765

1 All distances are given in inches and should be kept within a tolerance of +/- 0.01 inches

8. SDRAM Component Specifications

The 100 MHz SDRAM components used with this DIMM design spec MUST adhere to the latest revision of the Intel “PC SDRAM” Specification for operation of 100 MHz SDRAM devices. Please reference this document for all technical specifications and requirements for such devices. Any violation of the requirements of the Intel PC SDRAM component spec constitute a violation of the 100 MHz registered DIMM specification as well.

9. EEPROM Component Specifications

The Serial Presence Detect function MUST be implemented on the PC SDRAM Registered DIMM. The component used and the data contents must adhere to the most recent version of the Intel PC SDRAM Serial Presence Detect Specification. Please reference to that document for all technical specifications and requirements of the serial presence detect devices. Any violation of the requirements of the Intel PC SDRAM Serial Presence Detect specification constitutes a violation of the PC SDRAM Registered DIMM Specification as well.

10. Register Component Specifications

The following components are recommended for registers for the 100MHz register DIMM:

Manufacturer	Part Number	
TI / Hitachi	74ALVC162835	18Bit, 1:1 Register (w/internal damping resistors)
Hitachi	74ALVC16835	18Bit, 1:1 Register

Please reference the data sheets for the above parts for all technical specifications and requirements.

Below is a chart explaining which registers are used on which DIMMs.

DIMM	REGISTER	QTY
512MB	162835	3
256MB	162835	3
128MB	16835	2
64MB w/PLL	162835	2
64MB wo/PLL	162835	2

Figure 31: DIMM Register Use

The following specifications for the registers are critical for proper operation for the registered DIMM. These are meant to be a subset of the parameters for the device, but must be met if a different, but functionally equivalent, part is to be used.

Device	Parameter	From (input)	To (output)	Vcc = 3.3V ± 0.15V 0-65°C		Units
162835	T_{pd}	Clock	Y	Min 1.9*	Max 4.5*	ns
16835	T_{pd}	Clock	Y	Min 1.7*	Max 4.5*	ns

- T_{pd} times are measured into a 50pF load.

Device	Parameter	Conditions	Vcc = 3.3V ± 0.15V 0-65°C	Units
162835	I_i	V_i =0 to 3.45V	Max 10	µA
16835	I_i	V_i =0 to 3.45V	Max 10	µA

The following IV characteristics must be met, along with the above parameters to meet the requirements of this specification.

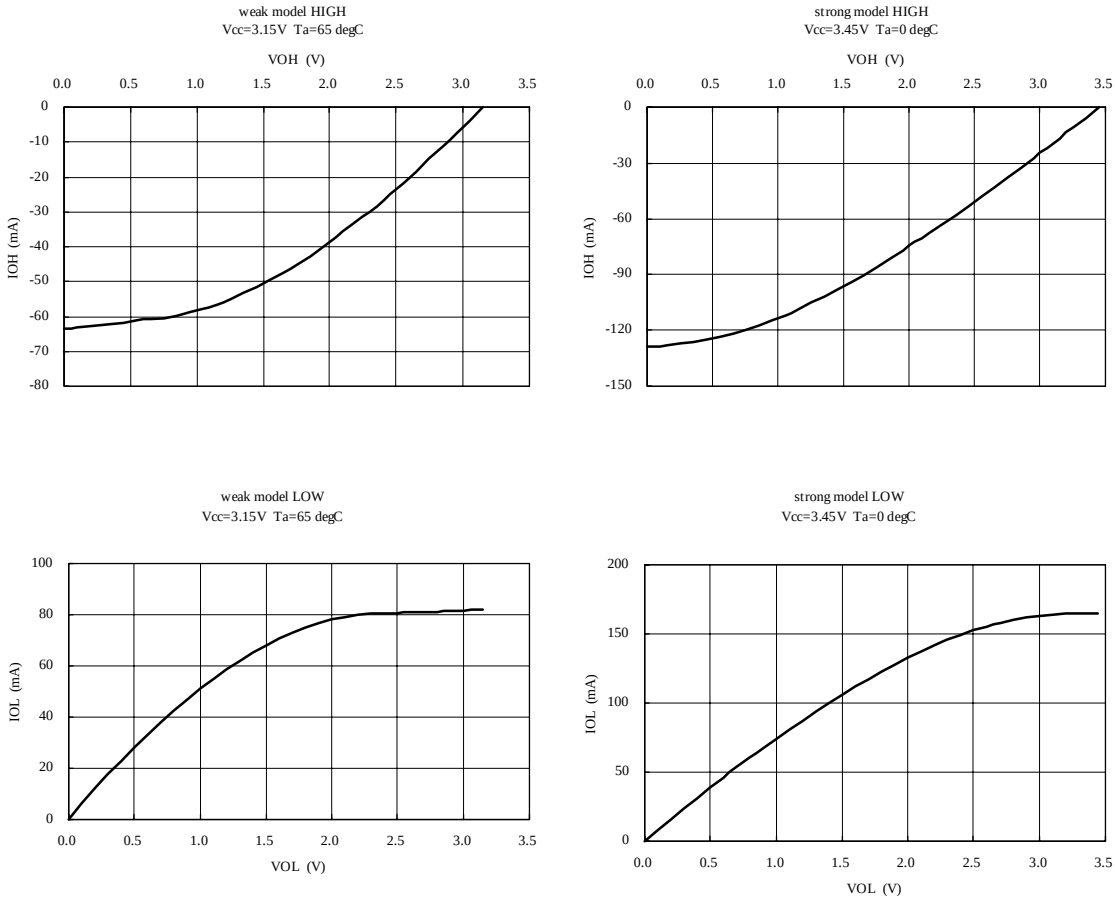


Figure 32: IV Characteristics for 16835 Register Output

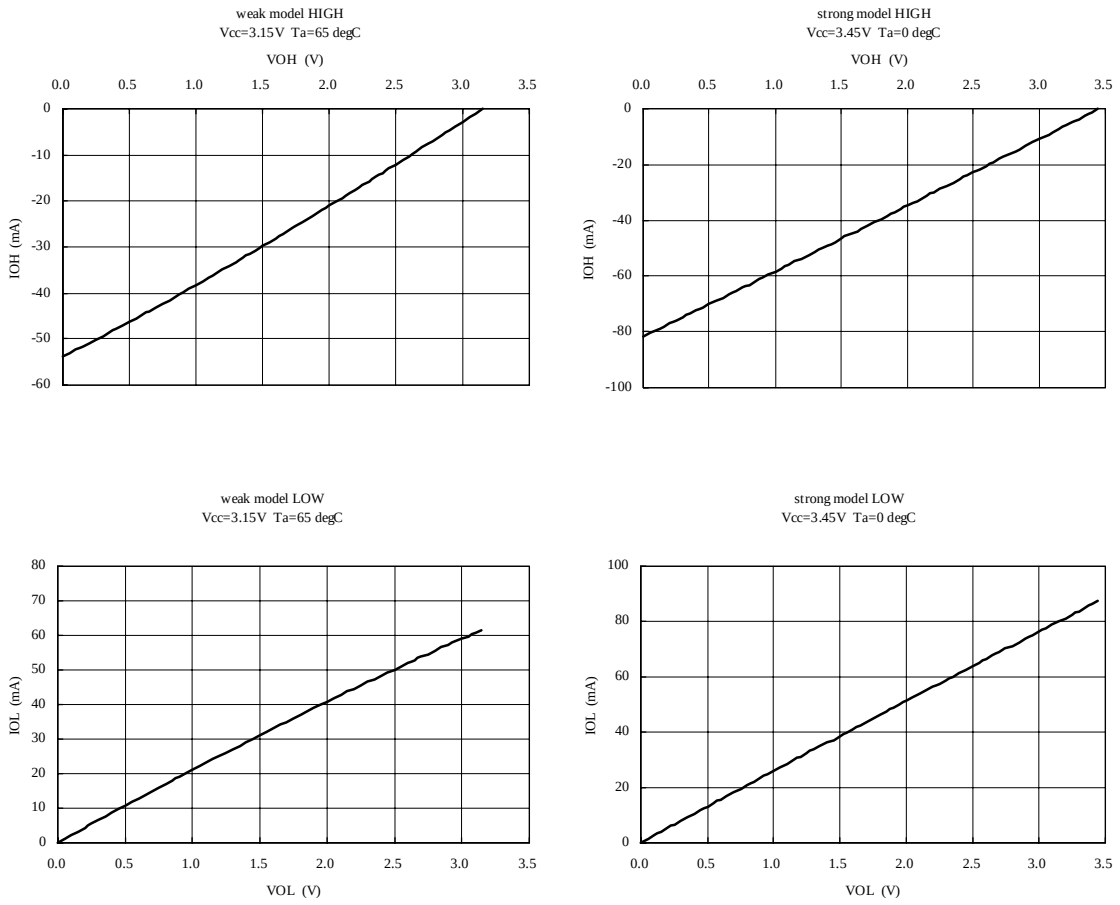


Figure 33: IV Characteristics for 162835 Register Output

11. PLL Component Specifications

The following components are recommended for the PLL for the 100MHz registered DIMM:

Manufacturer	Part Number	
TI	CDC2509A	1:9 PLL Based Clock Driver
TI	CDC2510A	1:10 PLL Based Clock Driver

Please reference the data sheets for the above parts for all technical specifications and requirements.

Below is a chart explaining which PLLs are used on which DIMMs.

DIMM	PLL
512MB	CDC2510A
256MB	CDC2510A
128MB	CDC2509A
64MB w/PLL	CDC2509A
64MB wo/PLL	NA

Figure 34: DIMM PLL Use

The following specifications for the PLL are critical in proper operation for the registered DIMM. These are meant to be a subset of the parameters for the device, but must be met if a different, but functionally equivalent, part is to be used.

Device	Parameter	From	To	Vcc = 3.3V ± 0.15V 0-65°C	Units
CDC2509A CDC2510A	Jitter	Output in CLK n	Output in CLK n+1	+/- 100	ps
CDC2509A CDC2510A	SSC induced skew *	Output in CLK n	Output in CLK n+1	+/- 200	ps
CDC2509A CDC2510A	Skew	Output	Output	200	ps

* SSC Induced Skew: SSC stands for Spread Spectrum Clock. The use of SSC synthesizers on the system motherboard will reduce EMI. The PLL used on the registered DIMM needs to support SSC synthesizers with the following parameters:

	Min	Max	
Modulation Frequency	30KHz	50KHz	
Clock Frequency Deviation		0.5%	(ex. for 100 MHz: 99.5MHz to 100MHz range)

PLL designs should target the values below to meet the 200ps maximum of SSC induced skew:

Greater than 1.2MHz PLL loop bandwidth

Less than -0.031 degrees of phase angle

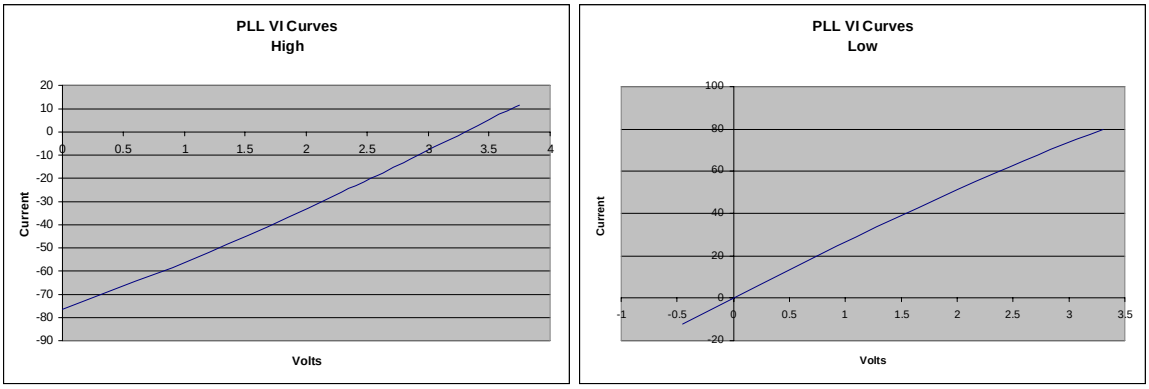


Figure 35: IV Characteristics for PLL Output